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(71) Applicant *(for all designated States except US)*: NETWORK EXPRESS [US/US]; 2200 Green Road, Ann Arbor, MI 48105 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)* : BUTLER, Timothy [US/US]; 1441 Natalie Lane #122, Ann Arbor, MI 48105 (US). CARSON, David, J. [US/US]; 325 Hilldale, Ann Arbor, MI 48105 (US). DEVRIES, Paul, A. [US/US]; 38534 Laurenwood Dr., Wayne, MI 48184 (US). ILIEV, Simeon [US/US]; 5907 Shagbark Dr., Ann Arbor, MI 48105 (US).

(74) Agent: ZIEGLER, Thomas, K.; Dykema Gossett, 400 Renaissance Center, Detroit, MI 48243 (US).

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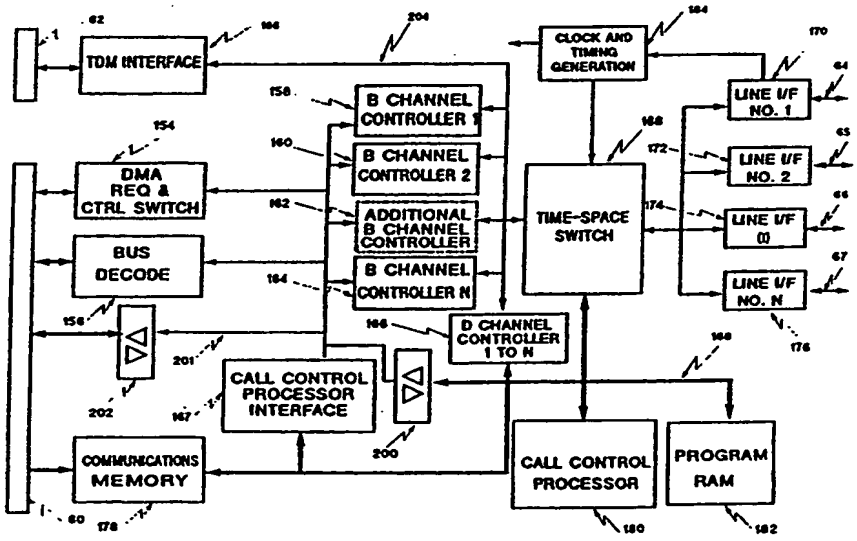

(57) Abstract

The invention uses a scheme of inverse multiplexing whereby a high bandwidth information stream (204) is first split into multiple narrow band signals for transmission through a public switched digital network over a plurality of narrow band channels (64, 65, 66, 67) to be received at the remote location by another Switched Network Access System then recombined to form the original high bandwidth information stream. The bidirectional direct memory access (DMA) request and control switch (154) of the present invention accepts requests for service from a plurality of peripherals, such as B-channel controllers (158, 160, 162, 164), then selects and assigns the requests on a call-by-call basis to any one of a plurality DMA requests lines utilizing a programmable DMA assignment register.

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SYSTEM FOR INTERNETWORKING DATA TERMINAL EQUIPMENT THROUGH A SWITCHED DIGITAL NETWORK

Field of the Invention

The present invention relates to a system for interconnecting pluralities of communication stations such as Personal Computer Local Area Networks (PC LANs) via access to Public Switched Digital Networks (PSDNs) provided by common carriers such as inter-exchange carriers, local exchange carriers and foreign national telephone companies. More particularly, the invention relates to a customer-premise-based system for internetworking data terminal equipment through a switched digital network and a related method for providing a virtual wideband network using a plurality of narrow band channels. The related method converts LAN and terminal destination addresses into telephone numbers then establishes multiple call connections to multiple remote destinations through both PSDNs and/or dedicated private line networks while performing dynamic bandwidth allocation and adjustment between end points based on predetermined channel utilization criteria.

The present invention also relates to an apparatus and method for control of direct memory access (DMA) data transfer. More particulary, a direct memory access request and control switch maps channels between a data memory and a plurality of B-channel controllers which transmit data from one communications switching node to the next. The direct memory access request and control switch assumes responsibility for the control of bit and byte data transfer, off-loading this task from the main CPU.

The present invention also relates to an apparatus and related method for synchronizing the Switched Network Access System to the Public Switch Digital Network. More particularly

the invention relates to an apparatus and related method for deriving a master clock from the framing sequence of the highest of the several possible orders of communication lines connected to the Switched Network Access System.

Background Art

In the 1980's there was a proliferation of personal computers and workstations interconnected by LANs which allowed local users to share resources. However, LAN growth during the 1980's was unpredictable and provincial creating, in the 1990's, the need to develop Wide Area Networks (WANs) to internetwork LANs allowing users to organize, manage and rapidly access distributed information resources. WANs provide a bridge between the PC/LAN environment, high performance terminals, work stations and the large host environment. WANs give PC users access to remote high bandwidth applications such as imaging, CAD/CAM (Computer-Aided Design/Computer-Aided Manufacture) and data base management. The inability of telecommunications facilities thus far to meet the high bandwidth availability and reliability requirements of new computer applications, which manipulate ever increasing amounts of information, has been a barrier to the development of WANs.

In the past, others have attempted to combine several narrow band channels of the public switched network to form a wideband facility. These arrangements typically establish each narrow band channel independently, resulting in multiple transmission paths routed through different network equipment. Thus, each narrow channel may have a different physical length and therefore, a different propagation time or transmission delay. An arrangement embodying this approach is disclosed in U.S. Patent 4,577,312 issued on Mar. 18, 1986 to Nash. The system shown in Nash breaks a high bandwidth information stream into multiple streams, then transmits information simultaneously

over multiple narrow band channels finally reconstructing the original information stream at the receiving end. An associated phone set is used to establish each connection independently of the preceding paths. Transmission delay on each connection is measured by sending and receiving a test pattern. A compensating delay is inserted into each line so that information sent along each narrow band channel arrives with the appropriate time delay across all channels.

Establishing each narrow band transmission path independently proves troublesome because any central office in any of the multiple paths established may, at any time, generate a frame slip or extra bit in an attempt to maintain synchronization on one of the paths. When such a frame slip is generated, all relative time delays previously determined become invalid. New time delay parameters must be ascertained and the multiple channels re-synchronized thereby degrading network throughput performance. Resynchronization of the multiple channels in this scheme is difficult due to the unpredictable manner in which the frame slips are generated throughout an extensive network. The present invention is directed toward eliminating such deficiencies in prior systems.

SUMMARY OF THE INVENTION

The present invention provides a system architecture and related method for interconnecting communication stations such as PC/LANs via access to both PSDNs and dedicated private line networks. The present invention employs inverse multiplexing wherein a stream of high bandwidth data packets is first split into multiple narrow bandwidth packet streams for transmission through a public switched digital network over a plurality of narrow band channels. The data packets are received at a remote location by another Switched Network Access System and

recombined to form the original high bandwidth information stream. Inverse multiplexing causes multiple narrow band channels to appear as a single high bandwidth channel to high bandwidth end users. The present invention also provides automatic bandwidth allocation and agility, adding or dropping narrow band channels "as needed" based on user bandwidth utilization criteria to optimize throughput and reduce data communications costs.

The Switched Network Access System is immediately applicable to communications between remote high bandwidth users via both public switched digital networks and dedicated private line networks or any combination of standard communication services provided by common carriers.

Thus, according to one aspect of the present invention, a method is provided for transmitting high bandwidth data messages in the form of packets between user terminals via communication lines in a switched digital network which includes the steps of receiving packets of digital data, establishing a communication connection, identifying available time slots in the communication connections thus established, appending sequencing and routing information, then transmitting each of the packets in identified time slots.

According to another aspect of the present invention, a method is provided for transmitting high bandwidth messages between remote communication stations connected by a switched digital network which includes the steps of establishing a plurality of communication connections to a receiving station, forming each message into one or more packets of digital data, dividing each packet into a plurality of sub-packets, transmitting the sub-packets through the plurality of communication connections, receiving the sub-packets at the receiving end, then reassembling the sub-packets into packets.

According to another aspect of the present invention, an apparatus is provided for transmitting high bandwidth data messages in the form of packets between user terminals via communication lines in a switched digital network which includes a means for cross connecting data bits from any input time slot of a switching means for output onto any time slot of one or multiple channels, and a means for inverse multiplexing the data bits.

According to another aspect of the present invention, an apparatus and related method is provided for mapping channels between a data memory and B-channel controllers which transmit data from one communications switching node to the next. The apparatus includes a direct memory access request and control switch which utilizes an address pointer to locate data to be transferred in data memory in response to a request for more data from the assigned B-channel controller. B-channel controllers output bursts of data onto proper time slots on a TDM highway connected to a space-time-space switch which then transfers the data onto the proper communication line for transmission across the public switched digital network. The direct memory request and control switch achieves efficient data throughput and resource utilization for the Switch Network Access System.

According to another aspect of the present invention, an apparatus and related method is provided for synchronizing the Switched Network Access System of the present invention to the PSDN, in which a system master clock is derived from the framing sequence of the highest of the several possible orders of communication lines connected to the Switched Network Access System. A clock manager process running on the main CPU first arbitrarily selects a line interface to supply the system master clock then receives and administers state change indicators from a plurality of line interfaces. When state change indicators

reveal that a higher order communications line has become active, the clock manager process enables a digital phase lock loop (DPLL) on the corresponding line interface causing the line interface to output its derived clock to the TDM interface which distributes the derived clock to the entire Switched Network Access System. The clock manager process also ensures that a cut-over occurs when the active system master clock source is disconnected or becomes faulty.

It is therefore an object of the present invention to provide high bandwidth access to PSDNs to achieve global WAN interconnectivity thereby allowing PC and terminal users to share computing resources and gain access to information and high bandwidth applications which reside on remote hosts and servers.

Another object of the present invention is to reduce communication costs between LANs, terminals and workstations by providing bandwidth agility through dynamic bandwidth allocation on an "as needed" basis for each call session.

Another object of the present invention is to simplify internetworking between LANs, terminals and workstations by providing concurrent WAN connections and inverse multiplexing across a plurality of network services and network carriers.

Another object of the present invention is to meet high bandwidth communication facility requirements demanded by new asynchronous applications such as TI backup and peak overflow management.

A further of the direct memory access request and control switch of the present invention is to provide software management of direct memory access channel assignment on a call-by-call basis.

Another object of the direct memory access request and control switch of the present invention is to provide for cyclic scanning of peripherals for data transfer requests to service first-in-time requests first and for generation of interrupts when no direct memory access channels are available.

A further object of the direct memory access request and control switch of the present invention is to reduce component counts and circuitry based on a number of simplifying assumptions, while providing functionality similar to generalized direct memory access control circuits.

Other objects, features and advantages will become clear or will be made apparent during the course of the following description of the preferred embodiment of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a broad block diagram depicting a pair of Switched Network Access Systems of the present invention interconnecting remote high bandwidth application users via a public switched digital network.

FIG. 2 is a block diagram depicting the components of the Switched Network Access System shown in FIG. 1.

FIG. 3 is a block diagram depicting in the component parts of the system management processor shown in FIG. 2.

FIG. 4 is a block diagram depicting functional control entities residing on the system management processor shown in FIG. 3.

FIG. 5 is a block diagram depicting the component parts of device access shown in FIG. 2.

FIG. 6 is a block diagram depicting functional control entities residing on device access processor shown in FIG. 5.

FIG. 7 is a block diagram depicting the component parts of the network access shown in FIG. 2.

FIG. 8 is a block diagram depicting functional control entities which control the functioning of network access shown in FIG. 7.

FIG. 9 is a block diagram depicting components of the call control processor interface shown in FIG. 7.

FIG. 10 is a broad block diagram depicting the inputs and outputs to the direct memory access request and control switch shown in FIG. 7.

FIG. 11 is a schematic diagram of a generalized solution for the direct memory access transfer assignment.

FIG. 12 is a schematic diagram of the direct memory access request and control switch shown in FIG. 10.

FIG. 13 is a block diagram depicting the components of the CPE clock synchronization system shown in FIG. 7.

FIG. 14 is flow diagram tracing the steps of the method related to the CPE clock synchronization system.

FIG. 15 is flow diagram depicting method steps of the present invention.

FIGS 16A–16E are diagrammatic representations depicting appendage by multi-channel protocol of header information to the standard packet format for inverse multiplexing and sub-packet inverse multiplexing.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings wherein like reference numerals are used to reference identical components in various views, FIG. 1 depicts a pair of Switched Network Access Systems 30 providing high bandwidth user terminals, generally designated as 32-34, access to public switched digital network (PSDN) 36. High bandwidth users 32-34 include, by way of example, Ethernet-type LAN 38, token ring-type LAN 40, host computer 42, and data terminal 44. Users 32-34 access computer applications such as imaging, CAD/CAM, file transfer, and database management which require aperiodic high bandwidth data transmission between remote sites. PSDN 36 may be of a conventional type comprising, by way of example, local central office 46, remote central office 48, other central offices 50 and satellite links 52-54. Generally designated device access links 56-62, including LAN access links 56-58, connect high bandwidth user 32 or 34 to Switched Network Access System 30. Network access links, communication lines or channels 64-72, including switched network access links 64-68, connect Switched Network Access System 30 to PSDN 36. Communication lines as used in the specification means any type of telecommunication line, link or connection commonly provided by the Public Switched Digital Network.

Each Switched Network Access System 30, uses a scheme of inverse multiplexing by which a high bandwidth information stream is first split into multiple narrow band channels, transmitted through PSDN 36 over a plurality of narrow band channels to be received at the remote location by another Switched Network Access System 30 then recombined to form the original high bandwidth information stream. Switched Network Access System 30 causes multiple narrow band channels to appear as a single high bandwidth channel to remote high bandwidth users 32-34. Switched Network Access System 30 adds and drops

narrow band channels "as needed" based on user bandwidth utilization providing automatic bandwidth agility and allocation to optimize throughput and reduce data communications costs.

FIG. 2 depicts the primary components of Switched Network Access Systems 30 which include device access 74, network access 76, system management processor 78, address, data and control bus 80 and time division multiplex (TDM) bus 82.

Device access 74 provides user 32-34 with connectivity to Switched Network Access System 30 through any of three types of industry standard device access interfaces including LAN interface 84, terminal interface 86, and device interface 88. LAN interface 84 may include conventional Ethernet or token ring interfaces. Terminal interface 86 may include, by way of example, RS-232 and V.35 interfaces and device interface 88 may include standard synchronous and non-synchronous device interfaces.

Network access 76 includes switched network interface 90, dedicated network interface 92 and additional network interface 94. Switched network interface 90 includes, by way of example, interfaces which terminate ISDN, BRI and/or PRI lines. Dedicated network interface 92 may include standard interfaces to terminate T1 and leased lines. Additional network interfaces 94 may include interfaces to terminate DDS lines. Device access interfaces 84-88 permit a wide variety of user devices to connect to the Switched Network Access System 30 which provides users 32-34 with access to switched and/or dedicated private networks as well as to PSDN 36. All device access interfaces 84-88 and network access interfaces 90-94 described above are well known standards in the communications industry.

The system management processor 78 includes input/output controller 96, direct memory access (DMA) transfer controller 98, main CPU 100 and data memory 102, all of which form a standard PC platform as is depicted in greater detail in FIG. 3. The functional control entities depicted in FIG. 4 reside on system management processor 78 may be implemented by software if desired. These control entities include intelligent network management process 112 comprised of node topology management process 114, network topology management process 116 and connection management process 118. Additional control entities which perform system management include path manager process 120, clock manager process 122, multi-channel protocol process 124, defined by multiple B-channel driver process 126, and LAN bridge control process 128, defined by MAC WAN forward process 130.

FIG. 5 depicts device access 74 in which LAN interface 84, preferably Intel 82596CA, digital terminal interface 86, device interface 88, and local address memory 132, are connected via device access address, data and control bus 144 to device access processor 134, preferably Intel 80960CA, device access memory 136, input FIFO register 138, preferably Cypress CY7429, output FIFO register 140, preferably Cypress CY7429 and status and control register 142. All device access 74 components are conventional items, well known and readily available commercially to the public.

FIG. 6 depicts listening, learning, filtering, forward (LLFF) process 146 entities residing on device access processor 134 including source/destination learning process 148, filter process 150 and LAN/WAN forward process 152 which preferably implements IEEE 802.1 protocol for MAC (Media Access Control) layer bridges. Device access processor 134 under control of LLFF process 146, specifically source/destination learning process 148, monitors source and destination addresses inside

packets received through LAN access link 56. A local address table is compiled in local address memory 132 from responses monitored by source/destination learning process 148 on LAN access link 56.

Upon receipt of a data packet after learning has taken place, device access processor 134, under control of filter process 150, checks to see if the address is contained in the local address table in data memory 102. If the address is found, the address is local and the packet is discarded. However, if the address is not found in the local address table, the packet is assumed to be destined for a remote location and is transmitted via device access address, data and control bus 144 to output FIFO register 140 under the control of LAN/WAN forward process 152. Device address information is passed to main CPU 100 which compiles the information needed to generate a remote address table. At the direction of main CPU 100, input/output controller 96 forwards the remotely addressed packets from output FIFO register 140 to the data memory 102 via address, data and control bus 80. Intelligent network management process 112 then commands DMA transfer controller 98 to forward the remotely addressed data packets to the appropriate network access interface 90-94 via address, data and control bus 80. Filter process 150 also forwards any data packets with a destination address that explicitly identifies a bridge or contains a local group address.

FIG. 7 depicts, in further detail, the component parts of network access 76 shown in FIG. 1. Direct memory access request and control switch 154, and bus decode circuit 156, are connected via B-channel data bus 201 to B-channel controllers 158-164, preferably Seimens SAB82532, D-channel controller 166, preferably Seimens PEB2075, and call control processor interface 167. B-channel controllers 158-164 are connected via TDM highway 204 to space-time-space switch 168, preferably Seimens

PEB2055. The space-time-space switch 168 is also connected to line interfaces 170-176, preferably Seimens PEB2081. Space-time-space switch 168 is also connected via CPU data bus 188 to communications memory 178, preferably IDT 7133, call control processor 180, preferably Intel 80C186, and program RAM 182. Clock and timing generation circuit 184, which preferably includes Mitel 8941, is connected to space-time-space switch 168 and line interfaces 170-176. TDM interface 186 is connected via TDM Highway 204 to space-time-space switch 168.

Local 80186 16 MHz call control processor 180 manages all call control and protocols for OSI layers one, two and three that enable network access 76 to communicate across standard telecommunications services provided by PSDN 36 such as basic rate or primary rate ISDN. OSI layer one protocols specify electrical characteristics of the physical medium forming the telecommunications facility. Layers two and layer three enable call control processor 180, aided by call control processor interface 167, to initiate, establish, maintain and terminate connections with local central office switches located in central office 46 and remote central offices 48-50 within PSDN 36 in accordance with instructions received via communications memory 178 from main CPU 100. These instructions may include, by way of example, directions to establish a connection between Ethernet-type LAN 38 and host computer 42. To establish such a connection, packet address information is cross-referenced within communications memory 178 to a telephone number which is passed to call control processor 180 via CPU data bus 188. Call control processor 180 outputs the appropriate OSI layer two and three protocol signals to local central office 46 over communication lines 64-67 based on the access stimuli received from local central office 46.

FIG. 8 depicts WAN call control process for OSI layer two and three 206, the entity which controls the functioning of network access 76. WAN call control process for OSI layer two and three 206 includes time slot driver process 208, D-channel driver process 210, and layer one B-channel OSI layer one process 212. WAN call control process for OSI layer two and three 206 is responsible for the setup and release of switched data calls through PSDN 36.

To forward a remotely addressed data packet to the appropriate network access interface 90-94, main CPU 100 under the control of intelligent network management process 112 directs the transmission of the data packet from data memory 102 over address, data and control bus 80 to the appropriate B-channel controller 158-164. The data transfer rate is accommodated to the rate of the appropriate destination communication line 64-67. A pointer specifying the first address location in data memory 102 at which the data message is buffered is written into DMA controller 96. The pointer enables B-channel controller 158-164 to request information from data memory 102 as required by the communications line 64-67 rate. Data memory 102 responds by sending a burst of data to FIFOs within B-channel controller 158-164. B-channel controller 158-164 then forwards the data packet to space-time-space switch 168 at the appropriate communications line rate for transmission through the selected line interface 170-176 onto the communication line 64-67. Each line interface 170-176 is separately connected to the connection memory of space-time-space switch 168. All individual framing information delays are absorbed between line interfaces 170-176 and space-time-space switch 168. The B-channel side of space-time-space switch 168 is synchronous to a clocking signal derived from one of the communication lines 64-67 throughout the rest of the network access interface 90-94.

A unique feature of Switched Network Access System 30 results from the fact that each B-channel 158-164 and D-channel 166 controller is programmed to support the TDM protocol running on TDM highway 204. Each B-channel 158-164 and D-channel 166 controller is therefore able to transmit data of any bit length, starting in any time slot on TDM highway 204. For example, B controller 158-164 can be programmed to wait until time slot 12 and then send 8 bits. Thus, the present invention permits a call session established through a particular line interface 170-176 to be uniquely assigned to any B-channel time slot, time slot 12 for example, with the result that no other call session will subsequently be assigned to time slot 12 for the duration of the call session. In this way, contention management is controlled by software through the assignment of time slots for each call session.

Time slot assignment is administered by path management process 120 which is part of high level software running on main CPU 100. All B-channel controllers 158-164, contained in network access expansion cards 104-110, switch data onto the same TDM highway 204. Main CPU 100 is therefore able to assign, accept and transfer data from any device access interface 84-88, on any expansion card 104-110, onto any time slot for ultimate output to any communications line 64-67. This arrangement is unique in customer premise equipment in that a non-blocking cross-connection system, adaptive on a call by call basis, is provided between any user 32 connected to Switched Network Access System 30 and any communications line 64-72 via any TDM highway 204 time slot. The above described configuration provides users 32-34 with bandwidth agility, the ability to automatically increase bandwidth based on traffic demand, without manual reconfiguration. Although any B-channel 158-164 or D-channel 166 controller can be assigned to uniquely correspond to any line interface 170-176, at the same time, if two contiguous B-channel communications lines are provided from

PSDN 36, both can be assigned to the same B-channel controller 158-164. Thus, utilization of space-time-space switch 168 and high level time slot assignment administered by path management process 120 provides the flexibility of terminating either single or multiple contiguous DS0 channels on any one B-channel controller 158-164.

FIG. 9 depicts call control processor interface 167 defined by receiver 214, B-channel controller selector 216, driver 218, B-channel controller access state machine 220, B-channel data bus 201 and, data transceivers 200. Receivers 214 are non-inverting buffers which receive words of data via address, data and control bus 188 from system management processor 78. The receiver 214 outputs B-channel controller selection signals over lines 224-234 to B-channel controller selector 216, address words via driver-input lines 236-248 to drivers 218 and control signals via state machine input control lines 294-304 to controller access state machine 220. Drivers 218 are non-inverting buffers which output signals identical to the signals received when drivers 218 are active.

B-channel controller selector 216 utilizes logic circuits to decode and select the appropriate one of (4) B-channel 158-164 or the single D-channel 166 controller to receive information data based on the address portion of a data packet. Address information is input to B-channel controller selector 216 via B-channel controller address lines 224-234. Logic internal to B-channel controller selector 216 translates the input address data into an assigned B-channel controller 158-164. The internal logic within B-channel controller selector 216 determines which B-channel controller select line 250-256 to assert. At the same, data going to the determined B-channel controller 158-164 is placed on B channel data bus 201 under the control of controller access state machine 220. Thus, the data portion of an information packet is transmitted via

data transceivers 220 to FIFO registers internal to the selected B-channel controller 158-164.

Referring generally to FIGs. 2, 4, 7 and 9, main CPU 100 also programs B-channel controllers 158-164 with time slot assignments on TDM highway 204 to allow access to space-time-space switch 168. Once Switched Network Access System 30 has been initialized and is functioning in steady state, call management begins. As part of its assignment program, call control processor 180, keeps track of which time slot on space-time-space switch 168 has been assigned to transmit and accept data from which B-channel controller 158-164. Connection management process 118 running on system management processor 78 transmits the assigned time slot value to a time slot register internal to the B-channel controller 158-164. Once a data connection has been established, connection management process 118 no longer plays an active role. At call termination as the data connection is torn down, connection management process 118 again becomes active, interacting with B-channel controller 158-164.

Data is transferred, under the control of multi-channel protocol process 124, from data memory 102 residing on system management processor 78 to B-channel controllers 158-164. Data transfer occurs in both DMA transfer mode through direct memory transfer controller 98 or in interrupt mode through input/output controller 96. To resolve the access conflict which occurs when system management processor 78 tries to access a B-channel controller 158-164 already in DMA transfer mode, data transferred under the control of direct memory access request and control switch 154 is given higher priority. Call control processor interface chip select line (DMA transfer in progress) 222 is enabled to delay access to B-channel controller selector 216 until a DMA transfer in progress has been completed. Priority is given to DMA transfer controller 98 over interrupts

by call control processor 180 because establishment of new data calls can always be delayed by a few milliseconds or microseconds, but once a data channel is actively in DMA transfer mode, priority must be given to completing the transfer.

B-channel controllers 158-164 also accept data from call control processor 180 under the control of call control processor interface 167 creating another potential conflict in attempting to access a B-channel controller 158-164 already in DMA transfer mode. Therefore, additional arbitration is necessary. Data transceivers or isolators 200 create two data paths allowing call control processor interface 167 to arbitrate the conflict between call control processor 180 and system management processor 78 in accessing B-channel controllers 158-164. Data transceivers 200 are 16 bit bi-directional data buffers which are enabled to allow data to flow. When call control processor 180 transmits data to a B-channel controller 158-164, data transceiver 200 is enabled, and data transceiver 202 is disabled, allowing uninterrupted data flow from call control processor 180 to the appropriate B-channel controller 158-164. When system management processor 78 begins to transmit data to a B-channel controller 158-164, data transceiver 202 is enabled and data transceiver 200 is disabled allowing uninterrupted data flow from data memory 102 to the appropriate B-channel controller 158-164. By disabling and enabling data transceivers 200 and 202, controller access state machine 220 controls the bi-directional flow of data.

Bus decode circuit 156 is a standard ISA (Industry Standard Architecture) bus decoding circuit composed of gates, flip flops, timers etc. Bus decode circuit 156 performs a routing function for incoming data which is very similar to the routing function performed by B-channel controller selector 216 for outgoing data. Bus decode circuit 156 within each network access interface 90-94 decodes the address information to route

the data word to the specified destination B-channel controller 158-164 or communications memory 178. Based on the received address information, bus decode circuit 156 selects the appropriate destination device access interface 84-88.

As shown in FIG. 7, one side of TDM interface 186 is connected to TDM bus 82 and the other to TDM highway 204. Functionally, TDM highway 204 is organized as time slots which are synchronized to clock and timing generation circuit 184. Provision is made within TDM interface 186 to ensure that data assigned to particular time slots on TDM bus 82 are placed onto the proper time slot on TDM highway 204.

TDM bus 82 carries bi-directional traffic running between multiple network access interfaces 90-94, as distinguished from TDM highway 204 which, as its name implies, is a unidirectional "highway" with two separate "lanes" handing traffic which is going in opposite directions. Data from a single session going outbound on TDM highway 204 is placed on a time slot paired to receive the inbound responses from the same session. The time slot pair is treated as a single data session. Assignment of companion paths in opposite directions is made within TDM interface 186 by means of a secondary circuit which performs a switching function inside TDM interface 186.

In general, communications lines using a TDM protocol are unidirectional, point-to-point data applications in contrast to a bus protocol which implies a passive, non-directional protocol running on just a piece of wire. TDM interface 186 provides a transition or interface between the non-directional protocol of TDM bus 82 and the unidirectional path of TDM highway 204. A particular time slot pair on TDM highway 204 is assigned to correspond to a particular time slot on TDM bus 82 thereby providing switching functionality between the two traffic format schemes. TDM highway 204 conforms with standard TDM protocols

for time slot assignment to allow B-channel 158-164 and D-channel 166 controllers to access to space-time-space switch 168, which accepts the data from the time slots.

TDM interface 186 is a modified off-the-shelf component. One input to TDM interface 186 is the output from clock and timing generation circuit 184 which supplies synchronization for TDM interface 186. The clock lead on TDM interface 186 is bi-directional in that the lead can be configured either as an input or an output based on whether the line interface 170-176 selected as the master clock is local or on another network access interface 90-94.

FIG. 10 depicts input and output lines of direct memory access request and control switch 154 located on network access interface 90-94 within Switched Network Access System 30. A DMA transfer request received via one of (16) B-channel DMA request lines 306-336 is accepted, selected and assigned by direct memory access request and control switch and to one of (7) DMA request to system management processor lines 338-350 for transfer to system management processor 78. B-channel direct memory access request lines 306-336 are connected to B-channel controllers 158-164 located on the same network access interface 90-94. DMA transfer requests originate from any type of peripheral device connected to network access interfaces 90-94.

Direct memory access request and control switch 154 receives each DMA transfer request which is then routed to one of (7) DMA request lines 338-350 to system management processor 78. This one-to-one assignment is valid throughout the entire call session. Once the data call is terminated, the assigned DMA request to system management processor line 338-350 becomes an available resource to path management process 120 for service of future DMA transfer requests which may then be assigned (mapped or associated with or made to correspond) to a different

B-channel DMA request line 306-336. The one-to-one assignability between available B-channel DMA request lines 306-336 and available DMA request to system management processor lines 338-350 on a call-by-call basis is a novel feature of DMA request and control switch 154.

FIG. 11 is a schematic diagram of a generalized solution which could be implemented for any N X M (16 x 7, in the present case) DMA Transfer Assignment. DMA request and control switch 154 receives a DMA transfer request via one of (16) B-channel DMA request lines 306-336 connected to (7) (1 x 16) integrated selector circuits 398-410 which each have one B-channel DMA request selector output line 476. The signal transmitted on B-channel DMA request selector output line 476 is selected from among the (16) input values by writing the appropriate binary value into the corresponding DMA assignment register 412-426. B-channel DMA request selector output lines 476 are connected though logic gates 478-500 to (7) DMA request to system management processor lines 338-350 respectively. One of (7) DMA request to system management processor lines 338-350 is enabled by writing the appropriate binary value into DMA enable register 428 connected to logical gates 478-500. The described generalized DMA transfer assignment arrangement of FIG. 11 provides mapping of the value on any of (16) B-channel DMA request lines 306-336 onto any of (7) DMA requests to system management processor lines 338-350.

(7) DMA acknowledgement from system management processor lines 384-396 are connected to the inputs of (16) (1 x 7) integrated selector circuits 430-442. The DMA acknowledgement from system management processor selector output lines 502 of integrated selector circuits 430-442 are connected to B-channel DMA acknowledgement lines 352-382. DMA acknowledgement selection registers 444-474 are connected to corresponding (1 x 7) integrated selector circuits. An acknowledgement on any one

of (7) DMA acknowledgement from system management processor lines 384-396 is assigned for output onto any one of (16) B-channel DMA acknowledgement lines 352-382 by writing an appropriate binary value into the corresponding DMA acknowledgement selection register 444-474.

Although the generalized design depicted in FIG. 11 is a straightforward way to implement the assignment of any B-channel DMA request line 306-336 to any DMA request to system management processor lines 338-350 and the assignment of the returning DMA acknowledgement from any system management processor line 384-396 to any B-channel DMA acknowledgement line 352-382, the design occupies a great deal of space and fails to minimize the number of hardware components used. FIG. 12 represents DMA request and control switch 154 shown in FIG. 10 optimized for use in Switched Network Access System 30. DMA request and control switch 154 shown in FIG. 12 implements the functionality of the generalized DMA transfer assignment solution shown in FIG. 11, but does so in a more efficient manner which reduces the number of gates and registers required.

Referring to FIG. 12, a request for DMA transfer received via any one of (16) B-channel DMA request lines 306-336 is assigned to any one of (7) DMA request to system management processor lines 338-350 for transfer to main CPU 100 on system management processor 78. Incrementing scan counter 518, connected to (1 x 16) integrated selector circuit 398, sequentially selects one of (16) B-channel DMA request lines 306-336 for transfer as an input to request logical "and" gates 534-546. This scheme in effect sequentially scans (16) B-channel DMA request lines 306-336 for an active DMA transfer request for service.

Inputs of comparators 520-532 are each connected to both scan counter 518 and one of (7) corresponding DMA assignment registers 504-516. Comparators 520-532 compare two values and assert an output if the two values are equal. If the value in the scan counter 518 is equal to the value within the corresponding one of (7) DMA assignment registers 504-516, a match occurs and the output of the comparator 520-532 is asserted. For instance, if a value of (3) is placed in DMA assignment register 504, the output of comparator 520 is asserted when scan counter 518 reaches the value of (3). This scheme allows path manager process 120 to select which output of any one of (7) comparators 520-532 will be asserted based on the value of scan counter 518. Thus, the value of scan counter 518 selects which one of (16) B-channel DMA request lines 306-336 is asserted as the output of (1 x 16) integrated selector circuit 398. The output of each of (7) comparators 520-532 is connected to one of (7) DMA request to system management processor lines 338-350 via request logical "and" gates 534-546 respectively.

Request logical "and" gates 534-546 perform a logical "and" function with three inputs: the output value of (1 x 16) integrated selector circuit 398 which is selected from (16) B-channel DMA request line 306-336 by matching the value of scan counter 518, the output value of comparators 520-532 which are each asserted when a match occurs between the value of scan counter 518 and the programmed value of each corresponding DMA assignment register 504-516, and an enablement value from DMA enable register 548. Each of (7) request logical "and" gates 534-546 is connected to a corresponding one of (7) DMA request to system management processor lines 338-350. Logically "anding" the B-channel DMA request line 306-336 selected by scan counter 518 and the output of comparators 520-532 allows path manager process 120 to select any one of (16) B-channel DMA request lines 306-336 for output onto any DMA request to system management processor line 338-350. For example, if a value of

(7) is placed in the fourth DMA assignment register 510, the seventh request line or B-channel DMA request line 318 is mapped to the fourth DMA request to system management processor line 346. This scheme results in a very straightforward mapping of requests from (peripherals) B-channel controllers 158-164 onto address, data and control bus 80.

Assertion of any one of system management processor lines 338-350 stops scan counter 518 from scanning until the DMA request has been serviced. This enables only one DMA request to be made at one time, preventing contention for DMA service when more than one request is present. Even though may be a match between the scan counter 518 and the assigned B-channel DMA request line 306-336, path manager process 120 may elect not to use DMA transfer to service the request if the corresponding DMA request to system management processor line 338-350 has been reserved for DMA service on another network access interface 90-94. In this way, DMA enable register 548 allows path manager process 120 to allocate channels on address, data and control bus 80 among the various network access interfaces 90-94.

For a DMA request to be sent over address, data and control bus 80, there must be a comparator 520-532 match and a request for service. If the match is asserted on any one of (7) comparators 520-532 and no DMA request exits on the corresponding B-channel DMA request line 306-336, then a DMA request is not sent. When a DMA cycle of data transfer begins, one of 7 DMA acknowledgement signals 384-396 is asserted by DMA transfer controller 98. That signal is compared to the DMA request 338-335 which is active. If the channel numbers match a signal 222 is asserted from DMA Request and Control Switch 154 to call control processor interface 167 indicating that a DMA transfer is in progress. Call control processor interface 167 then asserts one of (4) B-channel select signals 250-256. DMA transfer controller 98 presents address information on address,

data and control bus 80 during DMA cycles which is intended to be used to selectively address devices during DMA transfers. The call control processor interface 167 uses that information to determine which one of (4) B-channel select signals 250-256 to assert. This select signal, in combination with signals on address, data and control bus 80, is presented to B-channel controllers 158-164. A feature of those devices allow them to use those signals to pass the DMA transfer data on the correct DMA channel. This eliminates the need for generating signals on B-channel DMA acknowledgement lines 352-382 through 1 of 7 select circuits 430-442.

A comparison between FIG. 11 and FIG. 12 shows that DMA assignment registers are common to both the generalized 412-426 and inventive 504-516 designs. DMA assignment registers map DMA requests received on B-channel DMA request lines 306-336 to one of (7) DMA request to system management processor 338-350. However, adding four bit scan counter 518 in FIG. 12 eliminates the need for (6) of the (1 x 16) integrated selector circuits 398-410 of the generalized solution shown in FIG. 11 so that only one (1 x 16) integrated selector circuit 398 is connected to (16) B-channel DMA request lines 306-336 in DMA request and control switch 154 as shown in FIG. 12. Thus, the addition of scan counter 518 to the logic scheme employed in DMA request and control switch 154 results in an overall reduction in the complexity of logic and significantly reduces the number of components utilized in achieving the same functionality as the generalized solution of FIG. 11.

A further reduction in the number of logic components is accomplished by eliminating the array of (16) (1 x 7) integrated selector circuits 430-442 in FIG. 11 based on the following simplifying assumption. Although there are more potential DMA transfer requests (#B-channels/network interface board x N interface boards) than available channels on address, data, and

control bus 80 to service these requests, only one DMA transfer request will receive service from DMA transfer controller 98 at any one time. When a DMA transfer request is received on any one of the (16) DMA request to system management processor lines 338-350, main CPU 100 must stop executing its program to relinquish control of data memory 102 before DMA request and control switch 154 may safely begin to read and write data into the appropriate memory block locations. Main CPU 100 transmits an acknowledgement to DMA transfer controller 98 indicating that it has stopped utilizing the applicable memory address block locations so that DMA request and control switch 154 may safely perform its data transfer. Therefore, an acknowledgement received by DMA request and control switch 154 from main CPU 100 can be logically associated with the immediately preceding request for DMA service received by DMA request and control switch 154. Thus, the general solution implemented in FIG. 11 which provides access for any B-channel DMA request line 306-336 to any DMA request to system management processor line 338-350 at anytime independently of access provided for assignment of any of (7) DMA acknowledgement from system management process lines 384-396 to any of (16) B-channel DMA acknowledgement lines 352-382 can be significantly simplified based on the assumption that an acknowledgment received on any of (7) DMA acknowledgment from system management processor line 384-396 is a response corresponding to the DMA transfer request immediately preceding that acknowledgement. Thus, all that is necessary to administer DMA acknowledgements is to ensure that an acknowledgment is sent.

Although up to 24 simultaneous call sessions can be established by space-time-space switch 168, only (7) seven active DMA requests can be serviced at any one time over address, data and control bus 80. Those service requests that cannot be assigned and serviced by DMA request and control switch 154 are handled by system management processor 78 by reading and writing into data memory 102 on an interrupt basis.

The benefit of dynamic assignment between B-channel DMA requests lines 306-336 and DMA request to system management processor lines 338-350 is realized if communication lines 64-72 are hyper-channels (lines of increased channel capacity such as H0, H1 or H15 lines added to the network topology by main CPU 100 under the direction of connection management process 118). Because the data rate on hyper-channels is much higher, data words must be accessed from both data memory 102 and accepted from the respective call control processor interface 167 driver-output data line 266-278 at a much higher rate. DMA transfer, because of the higher channel bandwidth, provides a method whereby Switched Network Access System 30 can keep pace with the increased data rate of hyper-channels.

Dynamic assignment permits allocation of DMA transfer resources such as DMA request to system management processor lines 338-350 to hyper-channels on a priority basis. If no hyper-channels are connected to the network topology, then communication channels 64-72 are assigned through DMA request and control switch 154 on a "round-robin" basis. Path manager process 120, running on main CPU 100 operates with a system wide view of Switched Network Access System 30 enabling path manager process 120 to allocate the internal resources of Switched Network Access System 30 so that as requests for DMA transfer service are received from B-channel controllers 158-164 on the various network access interfaces 90-94, intelligent network management process 112, which has a network-wide view, is able to request hyper channels to connect high volume user destination sites.

Network access interfaces 90-94 are received in expansion slots 104-110 to effect communication between DMA request to system management processor lines 338-350 on network access interfaces 90-94 and address, data and control bus 80. Address, data and control bus 80 is a standard ISA bus which may be found

within any PC or PC equivalent. DMA requests are transmitted from B-channel controllers 158-164 on each network access interface 90-94 via DMA transfer controller 98 to data memory 102. Address, data and control bus 80 carries three types of information. Address pointers which designate the first memory address location where a data block is located comprise the first type of information. The second type of information is data or the actual messages between users. Control messages which perform associated read/write requests, handshaking and for each communication line connected to line interfaces 170-176 and other protocol functions comprise the third type of information.

Network access interfaces 90-94 each have (16) B-channel DMA request lines 306-336 which contend for the same (7) DMA request to system management processor lines 338-350. System management processor 78, under the control of node topology management process 114, tracks not only which B-channel DMA request lines 306-336 have transmitted a DMA transfer request but also which network access interface 90-94 originated the request. System management processor 100, under the control of path manager process 120, allocates internal node resources for any particular connection by generating and manipulating a list or table of connections which associates each DMA transfer request with a network access interface 90-94, B-channel DMA request line 306-336, call control processor interface 167 driver-output lines 266-278, B-channel controller 158-164, time slot on TDM highway 204, and a line interface 170-176. Because path manager process 120 has a system wide view, this control entity is able to allocate internal resources for DMA transfer requests on a call by call basis.

Each network access interface 90-94 has a DMA request and control switch 154 with (7) DMA request to system management processor lines 338-350 competing for the (7) available channels

on address, data & control bus 80. Therefore contention exists among network access interfaces 90-94 for these (7) available channels. As a result of this contention, any particular network access interface 90-94 may have only two or three active call sessions which use DMA resources at any one time. Any additional call sessions will be handled by main CPU 100 using interrupts instead of DMA resources. Over time, the internal node topology of Switched Network Access System 30 varies as active call sessions are added and dropped. The changing node topology is tracked by path resource manager process 120 which administers or allocates internal resources to these call sessions.

Data transfer mode occurs after the establishment of a call session. During data transfer mode, B-channel controllers 158-164 request N bytes (for example 20), from an address location in data memory 102 specified by the address pointer. DMA transfer controller 98 on system management processor 78 accesses information stored in data memory 102. A DMA transfer request is received via the one of (16) B-channel DMA request lines 306-336 selected by scan counter 518. After receiving a request for data transfer, DMA transfer controller 98, under the control of multi-channel protocol process 124 (specifically B-channel driver 126), begins the transfer of 20 bytes of data stored in the consecutive data memory 102 locations beginning at the address location designated by the associated address pointer. Each B-channel controller 158-164 is connected to a corresponding B-channel DMA request line 306-336. Data received by B-channel controllers 158-164 from data memory 102 is then transmitted in multiples of 64 Kbps into particular time slots on TDM highway 204.

B-channel controllers 158-164 each have internal FIFO registers which provide for a small amount of data storage (for example, 20 bytes). Each B-channel controller 158-164 accepts

these 20 bytes at the very fast program rate (CPU clock cycle rate) then stores the 20 bytes in their FIFO registers for output on the assigned time slot of TDM highway 204 at the appropriate channel speed required by the particular communication line 64-67. Circuitry within each B-channel controller 158-164 periodically outputs data onto a time slot on TDM highway 204 then checks the FIFO register to request more data if the FIFO register is empty. Each B-channel controller 158-164 has two internal FIFO registers so that as one FIFO register is emptied the other FIFO register can be refilled providing a transparent process.

FIG. 13 depicts, in greater detail, CPE clock synchronization circuit 552 located on network access interface 90-94 including clock generation and control circuit 184. Clock generation and control circuit 184, connected between TDM highway 204 and line interfaces 170-176, includes digital phase lock loop (DPLL) 554 whose inputs are received from clock enablement register 558 and (1xN) integrated selector 556 which receives inputs from line interfaces 170-176 and clock enablement register 558. When enabled by clock manager process 122 residing on main CPU 100 via clock enablement register 558, clock generation and control circuit 184 delivers clocking signals generated by DPLL 554 to components within Switched Network Access System 30. Only one network access interface 90-94 will have an enabled DPLL 554 at any one time. Clock manager process 122 running on main CPU 100 selects which network interface 90-94 will synchronize the rest of the Switched Network Access System 30 by writing the appropriate binary value into clock enablement register 558 to enable network access select input 564.

Line interfaces 170-176 are standard components designed to interface with standard communications protocols which run on communication lines 64-67. Integrated circuits and an

associated crystal internal to standard line interfaces 170-176 output a clock regardless of whether communication lines 64-72 are connected to line interfaces 170-176 or whether a call session has been established between the line interface 170-176 and local central office 50. The internal clock within line interfaces 170-176 can be used to run Switch Network Access System 30 however, utilization of the internal clock would not synchronize Switched Network Access System 30 to PSDN 36.

Line interfaces 170-176 monitor framing sequences received on communications lines 64-67 respectively to determine whether the bit patterns violate the applicable communications protocol (rules such as "ones density" etc). The integrated circuit internal to the line interface 170-176 generates a control signal in response to framing sequence bit patterns that are in conformance with the communications line protocol. The control signals generated by line interfaces 170-176 are transmitted via space-time-space switch 168 to call control processor 180 to indicate whether synchronization has been achieved. Valid framing bit sequences are generated on the physical level (layer one) by corresponding remote line interfaces located at the local central office 46. Once synchronization has been achieved, the line interface 170-176 is ready to pass information over the communications line 64-67 in conformance with the communications protocol.

A communications line 64-67 may an active call session and a valid framing bit sequence but nevertheless not be following a valid level two protocol regarding the data transmitted across the communications line 64-67. According to the Basic Rate ISDN protocol, for example, a level two D-channel must be established between the local central office 46 switch and Switched Network Access System 30. Handshake commands from call control processor 180 are send back and forth across the communication line 64-67. If the active call session is supporting valid

level two data communications then a valid ISDN Basic Rate response will be received by call control processor 180 within the proper time period. If no second level response is received, call control processor 180 knows that a valid second level call session has not been established and can notify clock manager process 122 of this fact. However, the communications line 64-67 may still be used to derive the system clock master if electrical characteristics of the communications line 64-67 are good.

DPLL 554 is a standard 8941 DPLL Mitel Circuit. Frame pulses from the line interface 170-176 selected by (1xN) integrated selector 556 are accepted as input by DPLL 554. DPLL 554 utilizes the frames pulses from line interfaces 170-176 to generate synchronous clocks which it outputs, when DPLL 554 is enabled, to TDM highway 204. Utilizing its own internal high speed crystal, DPLL 554 produces or derives several other higher speed clocks, all synchronous to each other and to PSDN 36, based on basic frame pulse sequences provided by (1xN) integrated selector 556. DPLL 554 outputs two clocks, one of which is twice the rate of the other. Two other clocks are generated which are the inverse of these first two clocks. A frame pulse of 8KHz is also generated. DPLL 554 uses the frame pulse sequence of the selected line interface 170-176 to divide the its internal high speed crystal clock output yielding a synchronized 8 KHz pulse stream. At times DPLL 554 divides by slightly greater number, at other times by a slightly smaller number to maintain synchronization to the framing sequence it receives from the selected line interface 170-176.

(1xN) integrated selector 556 is a multiplexer having inputs from line interfaces 170-176 and clock enablement register 558. Clock manager process 122 running on main CPU 100 chooses which line interface 170-176 will transmit its framing sequence to DPLL 554 based on the value of line interface select

input 562 from clock enablement register 558. Only one input received from line interfaces 170-176 is selected for transmission to DPLL 554. All the other line interfaces 170-176 are ignored. (1xN) integrated selector 556 is a standard programable device called a FPGA (Field Programmable Gate Array) which is similar to a PAL (Programmable Array Logic) but contains more internal circuitry. The programming of a PAL is permanent in contrast to a FPGA which is reloaded every time the FPGA is powered up. Not only does the FPGA have a larger internal set of circuit components but changes can be made to clock generation and control circuit 184 simply by writing a new download program.

Output clock line 560 from clock generation and control circuit 184 is connected to TDM highway 204 and TDM interface 186 for distribution to all network access interfaces cards 90-94 for use as timing for all the other communication lines 64-67. TDM highway 204 generally includes clocking leads as well as leads utilized as data channels. Two different clocks rates are supplied to TDM highway 204. (three if the frame signal is included).

Once an active call session has been established between Switched Network Access System 30 and local central office 46, framing bits (one every 125 microseconds) are received from local central office 46. Line interfaces 170-176 synchronize their internal clocks to this framing pattern then transmit a state change indicator control signal to clock manager process 122 running on main CPU 100 via call control processor 180 indicating that the synchronization to PSDN 36 has been established. Clock manager process 122 running on the system manager processor 78 has a global view of all line interfaces 170-176 on network access interfaces 90-94 within Switch Network Access System 30. Clock manager process 122 selects the system master clock from among synchronized line interfaces 170-176.

Clock manager process 122, by writing the appropriate binary value into clock enablement register 558, enables both the line interface 170-176 and the network access interface 90-94 with the result that the synchronized line interface 170-176 is now supplying the system master clock for all bit level data clocking within Switched Network Access System 30.

Clock manager process 122 begins its selection of the system master clock by scanning a line interface table created by the programmer at installation time which defines the type of network access interfaces 90-94 installed in the particular Switched Network Access System 30. Types of network access interfaces 90-94 include, for example, T1, Basic Rate ISDN, or Primary Rate ISDN. Path manager process 122 enables the network access interface 90-94 with the highest order communication lines 64-67. For example, if a particular Switched Network Access System 30 was configured with both T1 and a Basic Rate ISDN network access interfaces 90-94, clock manager process 122 selects the T1 network access interface 90-94 because this card is connected to the fastest communications lines 64-67. The network access interface 90-94 selected may or may not have an active call in session to local central office 46.

Clock manager process 122 selects an active synchronized line interface 170-176 to supply the system master clock if the line interface 170-176 is of the proper level in the communication line 64-67 hierarchy. For instance, if clock manager process 122 "knows" from the installation configuration data table contained in data memory 102 that the particular Switched Network Access System 30 has a T1 line interface 170-176, clock manager process 122 will look for a T1 line interface 170-176 to become active. If after a pre-determined time no T1 line interfaces 170-176 become active, clock manager process 122 will select a lower order line interface 170-176 such as a basic rate ISDN line interface 170-176 as the initial system master clock.

Clock manager process 122 running on main CPU 100 maintains control over the selection of the system master clock from among the various line interfaces 170-176 on the various network access interfaces 90-94. Line interfaces 170-176 transmit state change control messages to call control processor 180 through space-time-space switch 168 which indicate which line interfaces 170-176 have synchronized to their respective communications lines 64-67. Call control processor 180 tracks, under software control, which line interfaces 170-176 are receiving valid framing sequences from their respective communication line 64-67 and are thus synchronized to PSDN 36. Call control processor 180 then signals clock manager process 122 when a line interface 170-176 has synchronized to PSDN 36.

At the present time, a fixed configuration of network access interfaces 90-94 is assumed and a list defining the protocol of network access interfaces 90-94 is pre-built at installation time into the node profile configuration tables in data memory 102. However, network access interfaces 90-94 do have an ID register which enables path manager process 122 to determine which type of card is present using the decode circuit 156. Automation of the creation of the installation configuration data table is an obvious improvement the Switched Network Access System. In the future, a program will query network access interfaces 90-94 to determine the protocol of each card based on information contained in an internal ID register to will build a configuration table.

Clock manager process 122 accesses the node profile configuration table and begins selection of the system master clock with the highest order or fastest rate communications line 64-67. For example, if one of the network access interfaces 90-94 is a T1 type, clock manager process 122 begins selection of the system master clock with this network access interface 90-94. If a communications line 64-67 on this T1 network access

interface 90-94 is active and a call session has been established then the choice is a good one. If not, clock manager process 122 selects a network access interface 90-94 with the next lower communications line 64-67. If all communication lines 64-67 connected to the particular Switched Network Access System 30, are of equal speed, clock manager process 122 proceeds round robin until an active communication line 64-67 is located.

When an active call session is established between a line interface 170-176 and the local central office 46, the line interface 170-176 will start generating a new clock. Call control processor 180 will inform clock manager process 122 that the communications line 64-67 has become active. A decision is made by clock manager process 122 whether to derive the system master clock from the new higher rate communications line 64-67. If the communications line 64-67 currently chosen as the system master clock looses synchronization, clock manager process 122 will choose another communications line 64-67 to become the system master clock. This change may result in a communications line 64-67 of a lower order being chosen as the system master clock. Ultimate control for the system master clock selection and distribution is the responsibility of clock manager process 122 running on the main CPU 100 which has a global view of all communications lines 64-67 on all the network access interfaces 90-94 connected to Switched Network Access System 30.

At initial power-up of Switched Network Access System 30, one DPLL 554 on one network access interface 90-94 is chosen to generate clocks even though none of the line interfaces cards 170-176 are synchronized to their respective communications lines 64-67 (none are receiving a valid sequence of framing bits from their respective communications lines 64-67) at this time. The DPLL 554 chosen will nevertheless generate a clock to run

Switched Network Access System 30 until an active communication line 64–67 is found. After a pre-determined time period, if the chosen communications line 64–67 has not achieved synchronization but another communications line 64–67 has, the synchronized communications line 64–67 line is chosen as the system master clock. When an active communication line 64–67 is found Switched Network Access System 30 is synchronized to this line. Thereafter, the decision to derive the system master clock from a different communications line 64–67 is made only after an arbitration process.

The operation of CPE Clock Synchronous System as depicted in the flow diagram of FIG. 14 will now be described with reference to aspects of the preceding drawings. The method of the present invention begins in power-up condition 566. In Step 568, clock manager process 122 running in main CPU 100 marks or initializes all the communications lines 64–67 "ineligible" in the communication line table (node configuration data structure) contained in data memory 102. Because a clock is need to access internal hardware components of Switched Network Access System 30, clock manager process 122 arbitrarily designates, in Step 570, one communication line 64–67 to provide the system master clock master. Arbitrary selection of a system master clock in Step 570 results in selection of a system master clock which is closely, but not exactly, synchronous to PSDN 36.

In Step 572, clock manager process 122 enables the selected line interface 170–176 to supply the system master clock by writing the appropriate binary values into clock enablement register 558. In Step 574, clock manager process 122 waits for any line interface 170–176 to transmit a state change indicator message that a line interface 170–176 is receiving a framing sequence from the opposite end. The first state change indicator message received by clock manager processor 122 from a line interface 170–176 via call control processor 180 will

indicate only that a line interface 170-176 is receiving a frame sequence from its remote end. A short time later another state change indicator message will be sent indicating that the integrated circuit internal to the line interface 170-176 now recognizes the frame sequence received as a bit pattern valid within its line protocol and therefore that synchronization of line interface 170-176 to its corresponding communications line 64-67 has been achieved. In Step 576, call process manager determines whether the active communications line 64-67 should be considered "eligible." If the answer to this inquiry is "yes," clock manager process 122 in Step 578 then marks this line interface 170-176 as eligible for use as a system clock master in the communications line table located in data memory 102.

Assuming that Switched Network Access System 30 has just been powered-up, in Step 580 the answer to the inquiry, "is this line already functioning as the system master clock" is "no". The clock manager process 122 then proceeds in Step 582 to the next inquiry as to whether the current system master clock is eligible. Again because the system has just been powered up the answer to this question is "no". Consequently, the clock manager process 122 branches to Step 584 and makes this state-changed line interface 170-176 the source of the new system clock master. In Step 586, the new system master clock is distributed to all line interfaces 170-176 on all network access interfaces 90-94 which are disabled thereby adopting the system master clock which was determined in Step 584. Clock manager process 122 then branches to Step 574 to wait for another state change on line interfaces 170-176.

If another line interface 170-176 signals a detected state change on its respective communications line 64-67 and clock manager process 122 determines in Step 580 that this line is already the system clock master, clock manager process 122 will

return to Step 574 to wait for another state change indicator from line interfaces 170-176. In Step 582, if clock manager process 122 determines that the current system clock master is eligible but that the state-changed communication line 64-67 has a higher order clock (faster communications line) then clock manager process 122 will proceed to Step 584 to enable this state-changed line interface 170-176 as the new system master clock. (state changes can happen in ISDN where the communications line goes from being eligible to still being eligible as part of the ISDN protocol) However, if clock manager process 122 determines in Step 582 that the current system master clock is derived from a higher order clock (faster communications line), then clock manager process 122 will return to Step 574 to wait for another state change indicator from line interfaces 170-176.

In Step 576, if clock manager process 122 determines that the line interface 170-176 currently supplying the system master clock has changed state because the communications lines 64-67 has gone bad, for instance the communications line 64-67 is no longer suitable for transmission due to damage from gophers, failed terminal switching equipment etc., clock manager process 122 will mark this line interface 170-176 as ineligible for use as the system clock master in Step 590. Clock manager process 122 determines in Step 592 whether the state-changed line interface 170-176 marked as ineligible in Step 590 was the already the system master clock. If the state-changed line interface 170-176 was not the system clock master, then clock manager process branches to Step 574 to wait again for another state change indicator message from line interfaces 170-176. If the line interface 170-176 marked ineligible in Step 592 was the system master clock, clock manager process 122 then determines in Step 594 whether there are other eligible line interfaces 170-176 from which to derive a system master clock. If there are no other eligible line interfaces 170-176, clock manager

process 122 returns to Step 574 to wait for a state-change indicator message from line interfaces 170-176. In Step 596, if another line interfaces has been marked as eligible, clock manager process selects the highest order clock (fastest communications line) as the new system master clock then proceeds, in Step 586, to enable this line interface as the new system clock manager.

The eligibility of any one of line interfaces 170-176 for use as a system clock manager is determined by the bit error rate on the respective communication line 64-67. This error rate may be tested for validity through the associated cyclical redundancy test (CRC) in the ISDN line protocol or through specially designed bits within the T1 superframe protocol. Communications lines running ISDN or T1 protocols can be placed into a number of states, only some of which result in a communications line 64-67 which is suitable for use as a system clock master.

The operation of Switched Network Access System 30 as depicted in the flow diagram of FIG. 15 will now be described with reference to aspects of the preceding drawings. Assume that user 32 wishes to complete a high bandwidth data call across PSDN 36 to user 34. The method of the present invention begins in idle condition 598 followed by a source/destination learning phase 600 triggered upon the arrival of a packet on LAN access link 56. Device access processor 134 searches the local address table compiled in local address table 132 in Step 602 to determine whether the specified destination address is contained therein. In the event that the destination address does not exist in local address memory 132, the packet is assumed to be destined for transmission over PSDN 36. LAN/WAN forward process 152 begins in Step 604 as device access processor 134 signals a request to main CPU 100 via address, data and control bus 80 using status and control register 142 that a WAN connection is

needed. LAN/WAN forward process 152 provides destination information to intelligent network management process 112 which checks remote address tables and network topology. In Step 606, main CPU 100, under the control of intelligent network management process 112, accepts this request and information initiating path management process 120, in Step 608, which reserves the internal resources required to complete the connection within Switched Network Access System 30. These resources include by way of example, B-channel controller 158, line interface 170 and a time slot within space-time-space switch 168 and on TDM highway 204.

In Step 610, main CPU 100, under the control of intelligent management process 112, signals call control processor 180, operating under the control of WAN call control for OSI layer two and three 206, to make a connection to the remote site. Path management process 120 passes packet destination address information (which has been cross referenced to a phone number in communications memory 178 tables) to WAN call control for OSI layer two and three 206 which proceeds to perform the protocol (e.g. ISDN) signal exchanges with local central office 46-50 necessary to establish a communications call connection over PSDN 36. If a connection is established in Step 612, call control processor 180, under the direction of WAN call control for OSI layer two and three 206, informs path management process 120 that the connection had been established. In Step 614, path management process 120 accepts the call completion acknowledgement from call control processor 180 which is operating under the control of WAN call control for OSI for layer two and three 206 and informs intelligent network management process 112 that a connection has been established triggering, in Step 616, main CPU 100 under the control of connection management process 118, to update the connection structure data on network topology, connectivity and available services in data memory 102 to include a listing of the new

communications connection to that remote site across the WAN. In the event that a connection is not established in Step 612, device access processor 134 discards the packet in Step 618 and returns to idle condition 598 to repeat the process thus far described.

In Step 620, intelligent management process 112 directs multi-channel protocol process 124 to oversee the transfer of data utilizing the particular internal resources reserved by path management process 120 in Step 608. DMA transfer controller 98, under the control of B-channel driver process 126, accepts the assignment of a B-channel controller 158-164 then oversees the transmission of a single packet which it distributes across one or multiple connections according to the appropriate communications line 64-67 protocol. In Step 622, multi-channel protocol process 124 accepts packet data frames from LAN bridge control process 128, specifically MAC WAN forward process 130. MAC WAN forward process 130, operating on DMA transfer controller 98, passes a data memory 102 address pointer to device access processor 134, functioning under the control of LAN/WAN forward process 152, required by DMA request and control switch 154 to transfer packet frames from LAN interface 84 via address, data and control bus 80 to the assigned B-channel controller 158-164.

In Step 624, channel utilization is monitored by multi-channel protocol process 124 which determines if more bandwidth is required. As long as existing bandwidth meets throughput criteria, multi-channel protocol process 124 continues data transfer until the entire packet message has been transmitted. Upon the completion of data transfer in Step 626, call control processor 180, under the control of WAN call control process for OSI layer two and three 206, terminates the connection at the direction of intelligent network management process 112. DMA transfer controller 98, under the control of

multi-channel protocol process 124, transmits a signal to intelligent network management process 112 in main CPU 100. Intelligent management process 112 then decides whether to disconnect the communications connection. In Step 624, if a determination is made that more bandwidth is required, multi-channel protocol process 124 returns to Step 604 by signalling a request to intelligent network management process 112 on main CPU 100 that another WAN connection through PSDN 36 is needed to the same destination.

In the alternative, if a determination has been made in Step 624 that more bandwidth is not required, a test is made in Step 626 to determine whether transfer of all packets addressed to the specified remote destination has been completed. While transfer is not complete in Step 626, the method branches back to Step 622 wherein DMA transfer controller 98 continues to transfer LAN packet data frames. The transfer loop of Step 626 is also followed in Step 628 if the packet destination address exists in remote address table compiled by network topology management process 116. Once multi-channel protocol process 124 determines that data transfer is complete, disconnection occurs in Step 630 and the Switched Network Access System 30 returns to idle condition 598.

FIG. 16A depicts packets 632 and 634, part of a high bandwidth stream of data packets of LAPB or LAPD format, with layer 2 standard packet header 636 information already contained therein. B-channel controllers 158-164, under the control of multi-channel protocol process 124, append MCP header 638 including packet sequencing and destination routing information to individual packets 632 and 634 to facilitate inverse multiplexing of the information stream by local Switched Network Access System 30 and to permit re-assembly of the stream of high bandwidth data packets by the remote Switched Network Access System 30 at the receiving end. FIG. 16B depicts a high

bandwidth stream of data packets being received on LAN access link 56 into Switched Network Access System 30. Switched Network Access System 30 inverse multiplexes the packets onto communications lines 64 and 66 by breaking apart the data packet stream into packets 632 and 634 then transmitting them different communications channels to the same destination site. If a packet fragment is received at the far end, DMA transfer controller 98 re-transmits the packet. If multiple packets arrive out of sequence, the remote DMA transfer controller 98 re-sequences them before sending them out onto the remote LAN.

FIG. 16C depicts packet 632 of LAPB or LAPD format. B-channel controllers 158-164, under the control of multi-channel protocol process 124, segments packet 632 into sub-packets 640, 642 and 644 appending MCP header 638, which includes sub-packet sequencing and destination routing information, to each sub-packet. Inverse multiplexing of the type performed on the packet level in FIG. 16B is depicted on the sub-packet level in FIG. 16D over, by way of example, three communications channels 64, 66 and 68. Performing sub-packet inverse multiplexing improves terminal response time by decreasing transmission delay of the entire packet by 1/3, in the present example, of the original transmission time.

FIG. 16E depicts sub-packet inverse multiplexing of the type performed on the packet level in FIG. 16D over, by way of example, two communications channels 64 and 66 of unequal bandwidth. B-channel controllers 158-164, under the control of multi-channel protocol process 124, append MCP header 638 to sub-packets 646 and 648 which are proportioned to the ratio between the unequal bandwidths of communications channels 64 and 66. Like sub-packet inverse multiplexing of equal bandwidth channels, sub-packet inverse multiplexing of sub-packets through communication channels of unequal bandwidth improves terminal response time by decreasing transmission delay of the entire

packet and allows intelligent network management process 112 to make efficient utilization of all time slots on all channels of the communication connections.

B-channel controllers 158-164, under the control of intelligent network management process 112, implement the scheme of packet and sub-packet inverse multiplexing through their ability to assign and switch data onto any time slot on TDM highway 204 yielding a customer premise based non-blocking switching system, traditionally found only in central office equipment. To accomplish the three types of inverse multiplexing schemes, B-channel controllers 158-164 perform switching functions under the control of multi-channel protocol process 124 operating on DMA transfer controller 98.

CLAIMS

1. A method for transmitting high bandwidth digital data information in the form of data packets between user terminals via a plurality of communication lines in a switched digital network, comprising the steps of:

(A) receiving packets of said digital data information from a calling user terminal, said packets having a preselected sequence representing a correct message destined to be received by receiving user terminal via said communication lines;

(B) establishing a communication connection having a plurality of time slots through at least one of said communication lines over which said data packets received in step (A) may be transmitted to said receiving user terminal;

(C) identifying available time slots in the communication connection established in step (B) in which said data packets received in step (A) can be transmitted;

(D) appending to each of said data packets sequencing and routing information including identification of said receiving user terminal; and

(E) transmitting each of said packets received in step (A) in said time slots selected in step (C) over the communication connection established in step (B).

2. The method of claim 1, wherein steps (A) through (D) are performed at the site of said calling user terminal.

3. The method of claim 1, further including the steps of:

receiving at said receiving user terminal, said packets transmitted in step (E); and

assembling said received packets into said preselected sequence.

4. The method of claim 3, further including the step of:

verifying that the destination identified in said sequencing and routing information appended to each of said packets in step (D) matches said receiving user terminal.

5. The method of claim 1, wherein step (B) is performed by:

determining whether a communication connection has been previously established between said calling user terminal and said receiving terminal; and

establishing additional ones of said communication connections through additional communication connections in the event that an available time slots in said one communication session cannot be identified in step (C).

6. The method of claim 1, further including the steps of:

generating a record of said communication connections established; and

updating said record in response to a change in the number of said communication connections established in step (B).

7. The method of claim 5, including the step of:

reducing the number of said communication connections established when the available number of said time slots exceeds a preselected value.

8. The method of claim 1, further including the step of:

dividing each of said data packets into two or more sub-packets, and

appending to each of said sub-packets said sequencing and routing information.

9. The method of claim 8, wherein steps (C) and (E) are performed by:

identifying available time slots in said communications connection established in step (B) on a single one of said communication lines; and

transmitting said sub-packets over said one communication line.

10. The method of claim 8, wherein step (C) is performed by:

identifying time slots in a plurality of said communication lines, and

transmitting said sub-packets in time-slots over each of the communication lines in said plurality thereof.

11. A method for transmitting high bandwidth messages between remote communication stations connected by a switched digital network, comprising the steps of:

(A) establishing, at a sending communications station, a plurality of communication connections through said switched digital network to a receiving communications station;

(B) forming each of said messages into one or more packets of digital data;

(C) dividing each of said packets into a plurality of sub-packets;

(D) transmitting said plurality of sub-packets respectively through said plurality of communication connections to said receiving communication station;

(E) receiving said plurality of sub-packets at said receiving station; and,

(F) reassembling each of said plurality of sub-packets into packets at said receiving station.

12. The method of claim 11 wherein steps (B) and (C) are performed at said sending communications station.

13. The method of claim 11, wherein step (A) is performed by:

monitoring the bandwidth utilization of each of said communication connections to transmit said sub-packets, and

establishing additional ones of said communication connections when said utilization exceeds a first preselected value.

14. The method of claim 13, further including the step of:

disconnecting at least certain of said communication connections when said monitored utilization falls below a second preselected value.

15. The method of claim 11, further including the step of:

appending routing information to each of said sub-packets.

16. The method of claim 14, wherein step (C) is performed by:

assigning said sub-packets to certain time slots on a time division multiplex data highway; and

switching said sub-packets from said time division multiplex highway into available time slots on said

plurality of communication connections whereby bandwidth utilization of said communication connections is optimized.

17. The method of claim 16, wherein said assigning step is performed by:

associating each of said sub-packets with a controller functioning to output said sub-packet onto a certain one of said time slots; and

delivering each said sub-packet respectively to said associated controller.

18. A method of communicating high bandwidth digital data information between first and second local area networks (LANs), using a plurality of switched, narrow band communication connections and forming a wide area network (WAN), comprising the steps of:

(A) receiving frames of said digital data information from said first LAN, said frames having a preselected sequence representing a correct message to be transmitted through said WAN and received by said second LAN;

(B) establishing a first one of said communication connections in said WAN;

(C) transmitting over said first connection established in step (B) at least certain of said frames received in step (A);

(D) establishing at least a second one of said switched communication connections in said WAN when said level of bandwidth utilization exceeds a predetermined threshold;

(E) transmitting at least certain said frames over said second communication connection.

19. The method of claim 18, further comprising the steps of:

receiving at said second LAN, said frames transmitted over said first and second communication connections.

20. The method of claim 18 wherein step (C) is performed by:

providing a time division multiplexed (TDM) communication highway having a plurality of ordered time slots coupled to a means for uniquely assigning said frames to at least one of said ordered time slots, and a switching means coupled to said TDM highway, said switching means having a plurality of ordered input and output time slots for switching said frames from a particular ordered input time slot to a particular ordered output time slot associated with a ordered communications facility time slot;

receiving said frames in a preselected assignment means;

assigning said frames to a unique time slot on said TDM highway;

transmitting said frames in said assigned time slot to said switching means; and

switching said frames to a preselected switching means output time slot for output onto a preselected time slot on said ordered communications facility.

21. An apparatus for communicating high bandwidth data information in the form of packets between a first and a second local area network (LAN), using a plurality of switched, narrow band communication connections suitable for carrying voice messages, and forming a wide area network (WAN), comprising:

a time division multiplexed (TDM) communication highway having a plurality of ordered TDM time slots;

at least one controller means, coupled to said TDM highway, for uniquely assigning said data packets received from said first LAN to one of said ordered TDM time slots;

switching means, coupled to said TDM highway, said switching means having a plurality of ordered input and ordered output time slots, for switching said data packets from a certain input time slot to a certain output time slot; and

at least one communications connection, coupled to said switching means, for carrying the transmission of said data packets, said communications connection having a plurality of ordered time slots.

22. An apparatus for making connections for the transmission of data messages between a plurality of controllers and at least one communication connection in a switched digital network, each said connection having a plurality of communication channels in the form of fixed time slots, comprising:

system control means for monitoring said time slot utilization and for controlling the number of said communication connections established based on the level of time slot utilization.

23. The apparatus of claim 22, further comprising:

call control means, responsive to said system control means, for establishing or disconnecting said communication connections in response to signals from said system control means.

24. The apparatus of claim 23, further comprising:

connection means, responsive to said call control means, for providing a transmission path between said between said controller means and said communication connection;

routing means, coupled to said system control means and said connection means, for appending information to said data message, said information defining the sequencing and routing of said message;

25. In a telecommunications system, a method for transferring call messages defined by data bits between a data memory and a plurality of channel controllers under the control of a system processor, comprising the steps of:

(A) associating one of a plurality of direct memory access channels with one of said channel controllers at an initial call message set-up time;

(B) scanning said channel controllers for a request to transmit data;

(C) mapping said request onto one of said direct memory access channels; and

(D) transferring said data bits from said data memory to said one channel controller via said one direct memory access channel.

26. The method of claim 25, further comprising the step of:

(E) interrupting said system processor when no direct memory access channel is assigned to a channel controller requesting data transfer.

27. An apparatus for transferring messages in the form of data bits stored in addressed data memory locations between said data memory and at least one communication channel, said communication channel having a plurality of fixed time slots, comprising:

at least one channel control means for requesting and receiving said data bits from said data memory and for controlling the output of said received data bits onto said communication channel;

access control means, in communication with said channel control means, for controlling the association of said addressed memory locations with said data requests, said access control means having a plurality of channels for receiving and acknowledging said data requests; and

mapping means, connected to said channel control means and responsive to said access control means, for associating said data requests from said channel controller with one of said data request channels.

28. The apparatus of claim 27, wherein said channel control means are located on a plurality of circuit boards each connected to said access control means via at least one shared channel for receiving said data requests.

29. A method for synchronizing an internal timing source to the highest order timing source among a plurality of a communications connections, each said communication connection associated with an interface, comprising the steps of:

(A) scanning said plurality of interfaces for a first timing source; and

(B) synchronizing said internal timing source to the timing of said first timing source.

30. The method of claim 29, further comprising the steps of:

(C) scanning said interfaces for a second timing source; and

(D) synchronizing said internal timing source to said second timing source if said second timing source is of a higher order than said first timing source;

31. In a telecommunications system, an apparatus for synchronizing an internal timing source to the highest order timing source selected from a plurality of communication channels, comprising:

at least one interface means, connected to one of said plurality of communication channels, for generating a timing signal which is synchronized to said communication channel;

selection means, connected to said interface means, for selecting the highest order timing signal from among said plurality of communication channels; and

generation means, connected to said selection means, for generating a timing signal derived from said highest order timing signal.

32. The apparatus of claim 32, further comprising:

distribution means, connected to said generation means, for distributing said derived timing signal through said telecommunications system.

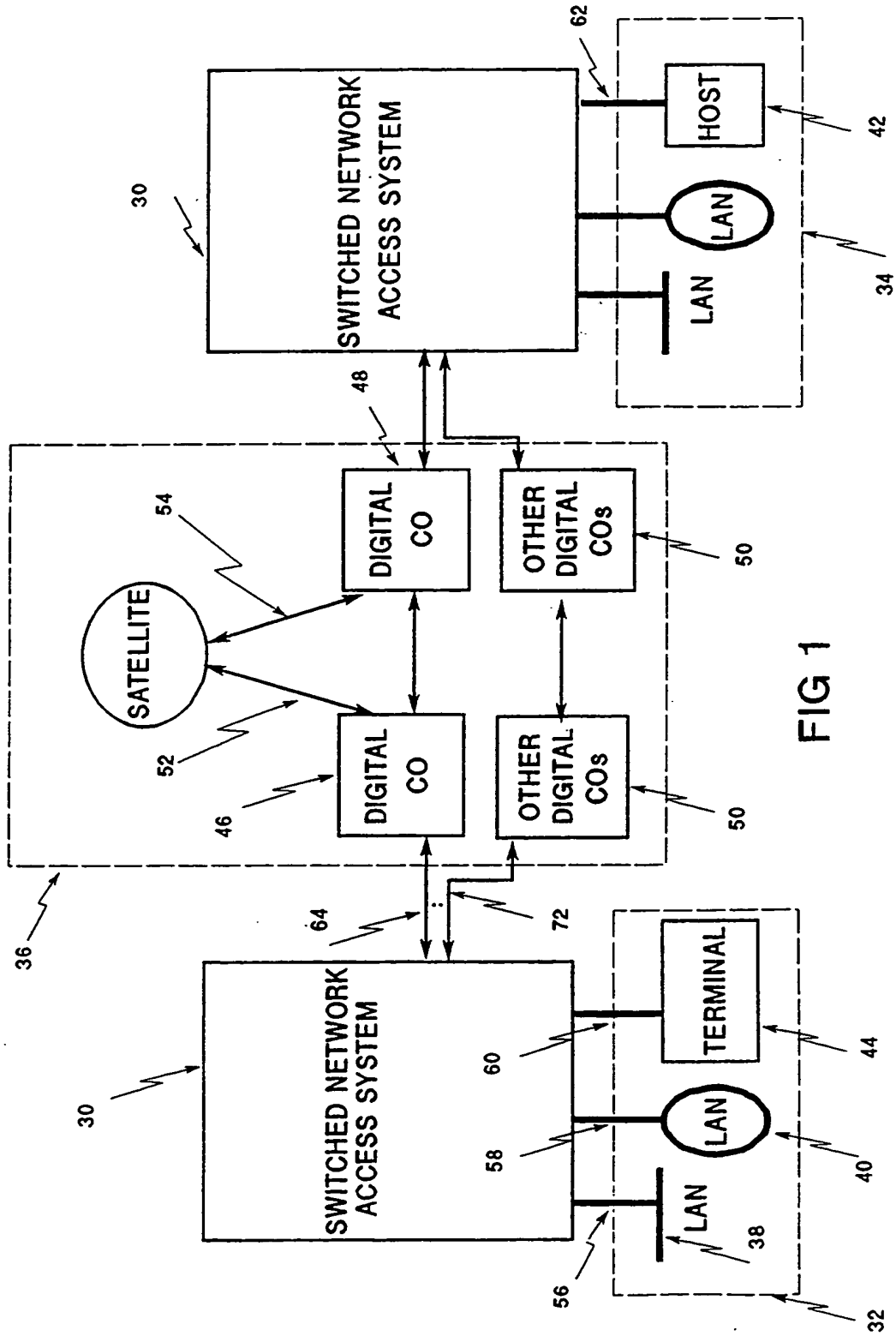

SWITCHED NETWORK ACCESS SYSTEM
30
62
HOST
42
LAN
LAN
34
48
DIGITAL CO
OTHER DIGITAL COs
50
54
SATELLITE
52
46
DIGITAL CO
OTHER DIGITAL COs
50
36
64
72
SWITCHED NETWORK ACCESS SYSTEM
30
60
TERMINAL
44
58
LAN
40
LAN
38
56
32

FIG 1

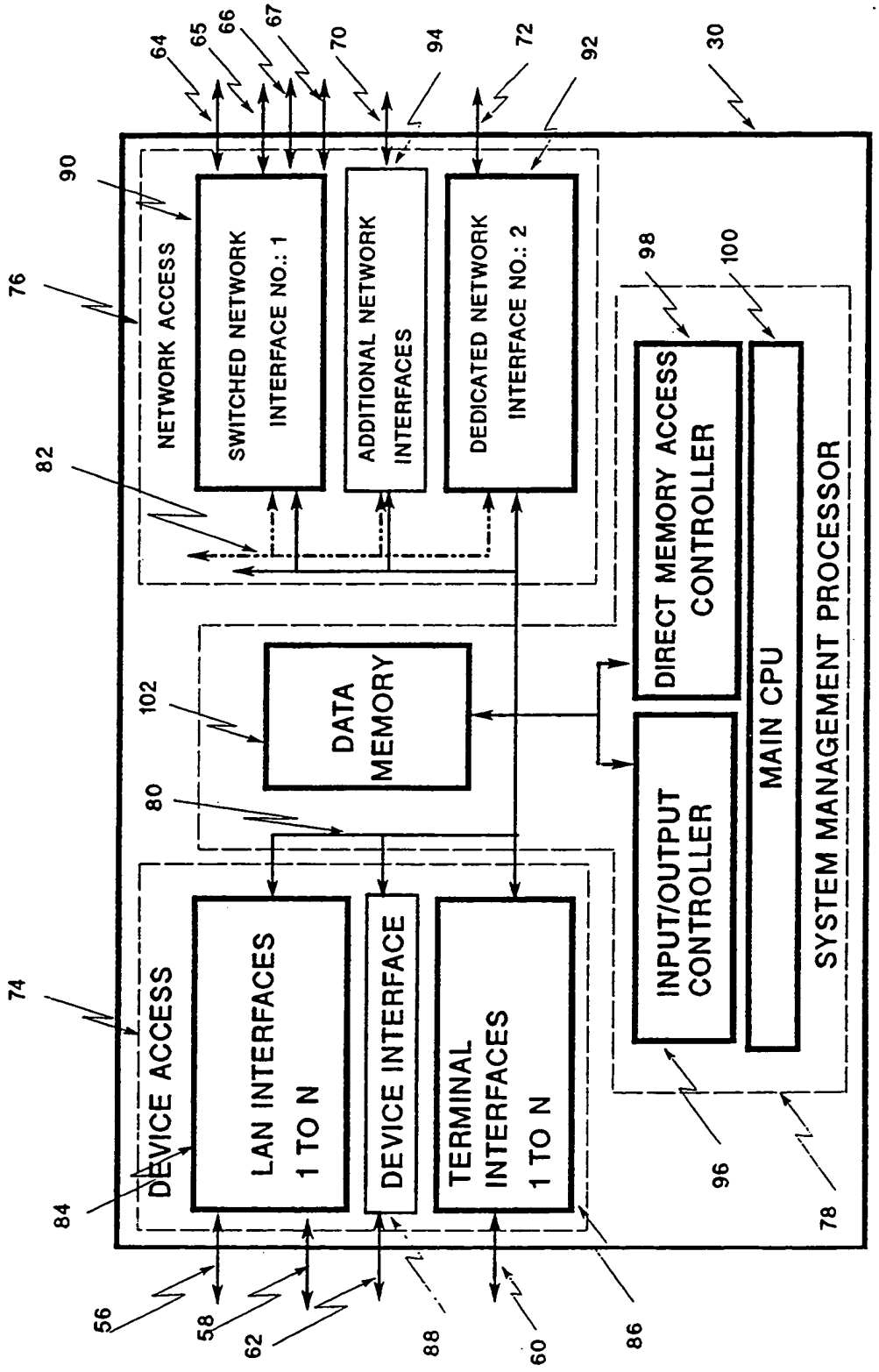

64
65
66
67
70
94
72
92
30
90
76
82
NETWORK ACCESS
SWITCHED NETWORK INTERFACE NO.: 1
ADDITIONAL NETWORK INTERFACES
DEDICATED NETWORK INTERFACE NO.: 2
98
100
DIRECT MEMORY ACCESS CONTROLLER
MAIN CPU
SYSTEM MANAGEMENT PROCESSOR
102
DATA MEMORY
80
74
DEVICE ACCESS
LAN INTERFACES 1 TO N
DEVICE INTERFACE
TERMINAL INTERFACES 1 TO N
INPUT/OUTPUT CONTROLLER
84
96
78
56
58
62
88
60
86

FIG 2

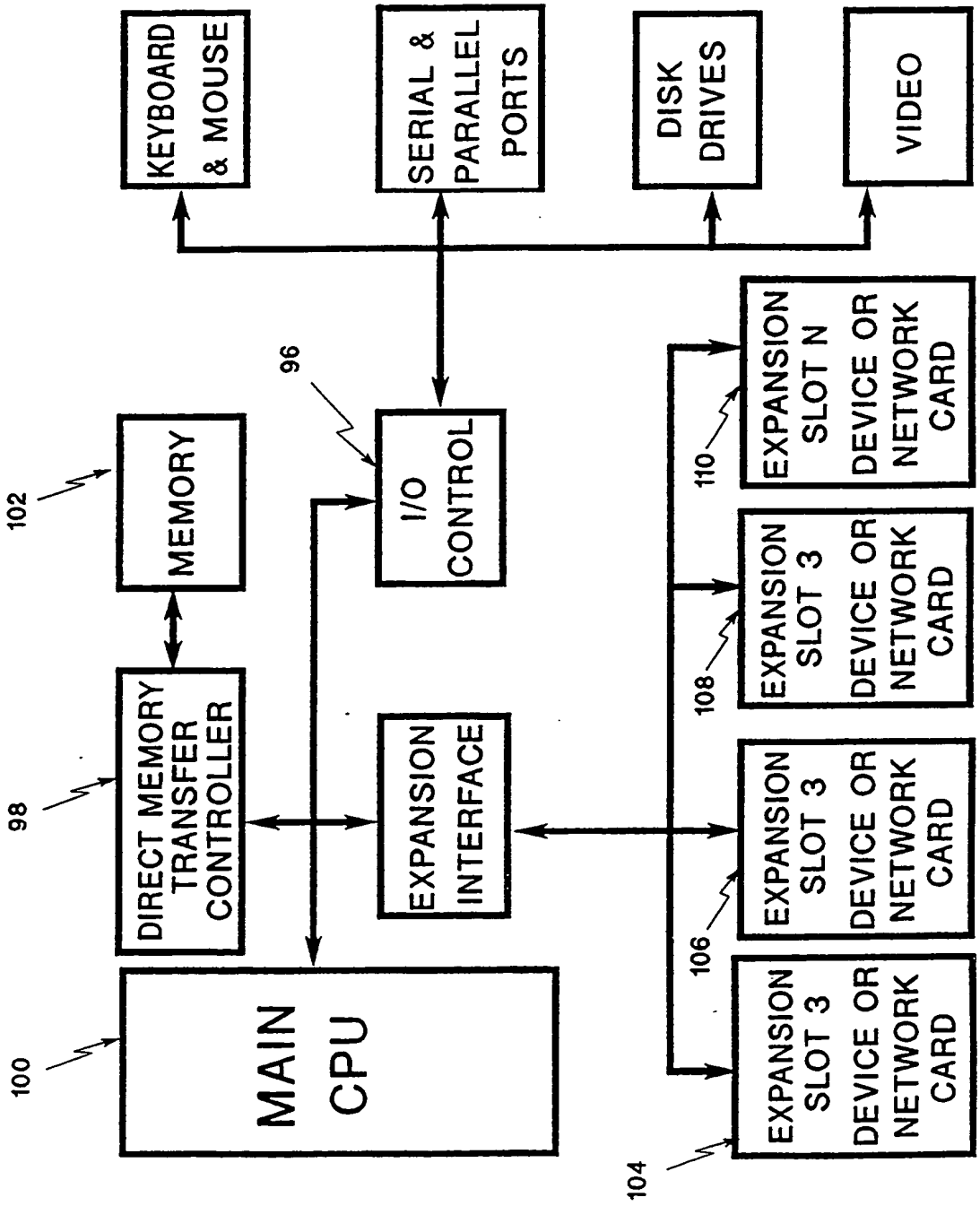

KEYBOARD & MOUSE
SERIAL & PARALLEL PORTS
DISK DRIVES
VIDEO
96
I/O CONTROL
102
MEMORY
98
DIRECT MEMORY TRANSFER CONTROLLER
EXPANSION INTERFACE
100
MAIN CPU
110
EXPANSION SLOT N DEVICE OR NETWORK CARD
108
EXPANSION SLOT 3 DEVICE OR NETWORK CARD
106
EXPANSION SLOT 3 DEVICE OR NETWORK CARD
104
EXPANSION SLOT 3 DEVICE OR NETWORK CARD

FIG 3

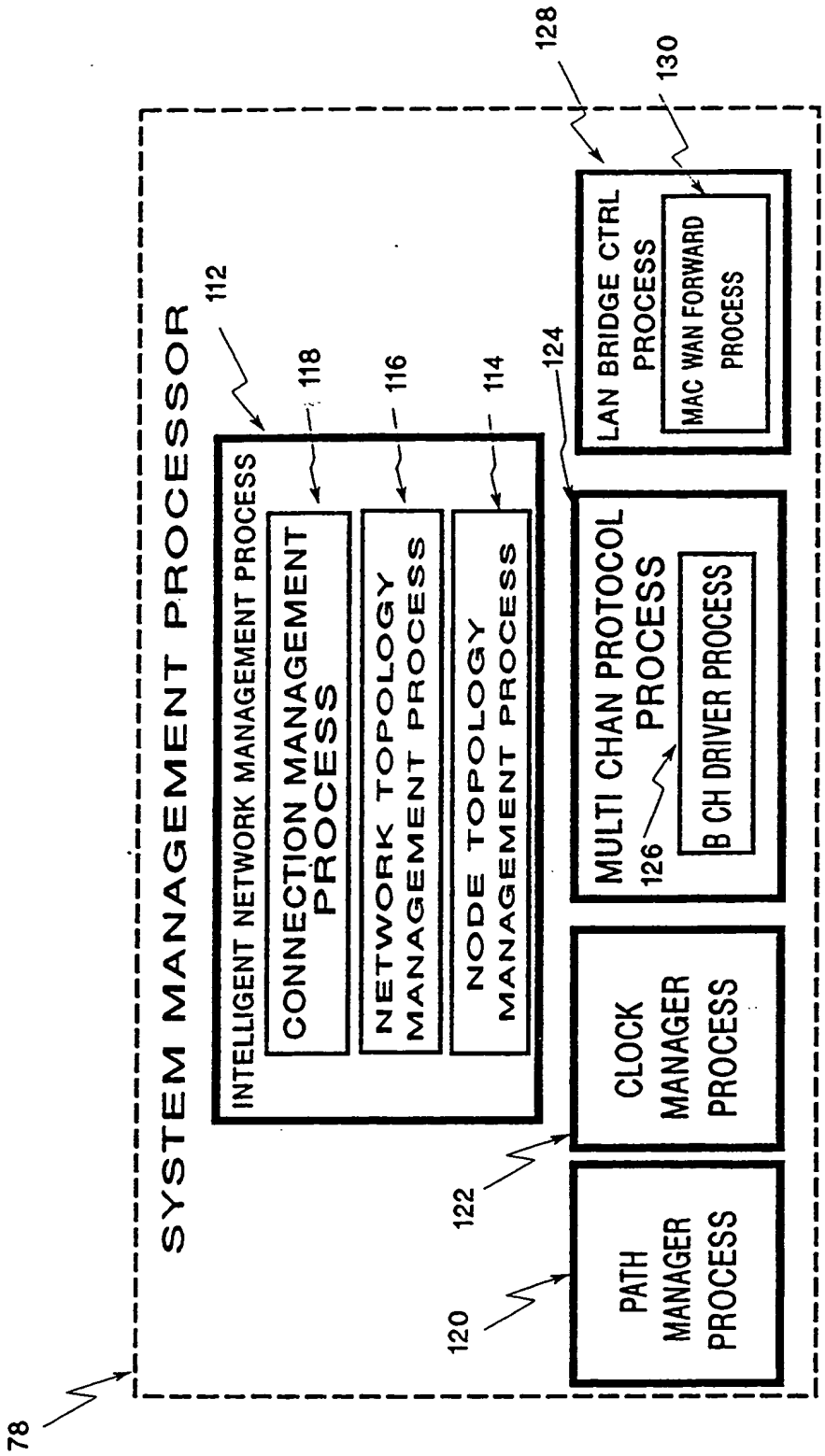

78
SYSTEM MANAGEMENT PROCESSOR
112
INTELLIGENT NETWORK MANAGEMENT PROCESS
CONNECTION MANAGEMENT PROCESS
118
NETWORK TOPOLOGY MANAGEMENT PROCESS
116
NODE TOPOLOGY MANAGEMENT PROCESS
114
124
MULTI CHAN PROTOCOL PROCESS
126
B CH DRIVER PROCESS
128
LAN BRIDGE CTRL PROCESS
130
MAC WAN FORWARD PROCESS
CLOCK MANAGER PROCESS
122
PATH MANAGER PROCESS
120

FIG 4

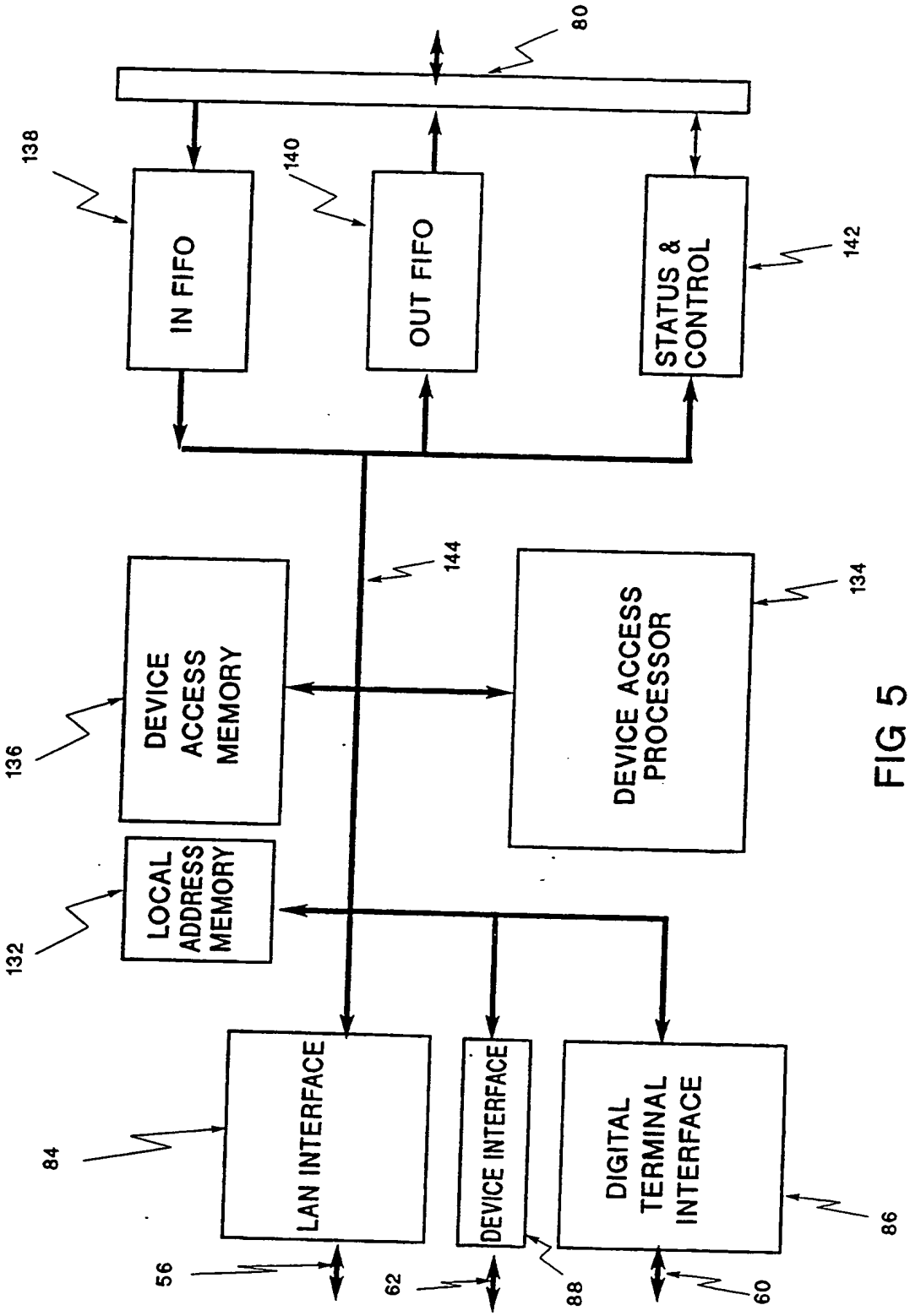

80
138
IN FIFO
140
OUT FIFO
STATUS & CONTROL
142
144
DEVICE ACCESS MEMORY
136
DEVICE ACCESS PROCESSOR
134
LOCAL ADDRESS MEMORY
132
LAN INTERFACE
84
DEVICE INTERFACE
DIGITAL TERMINAL INTERFACE
86
56
62
88
60

FIG 5

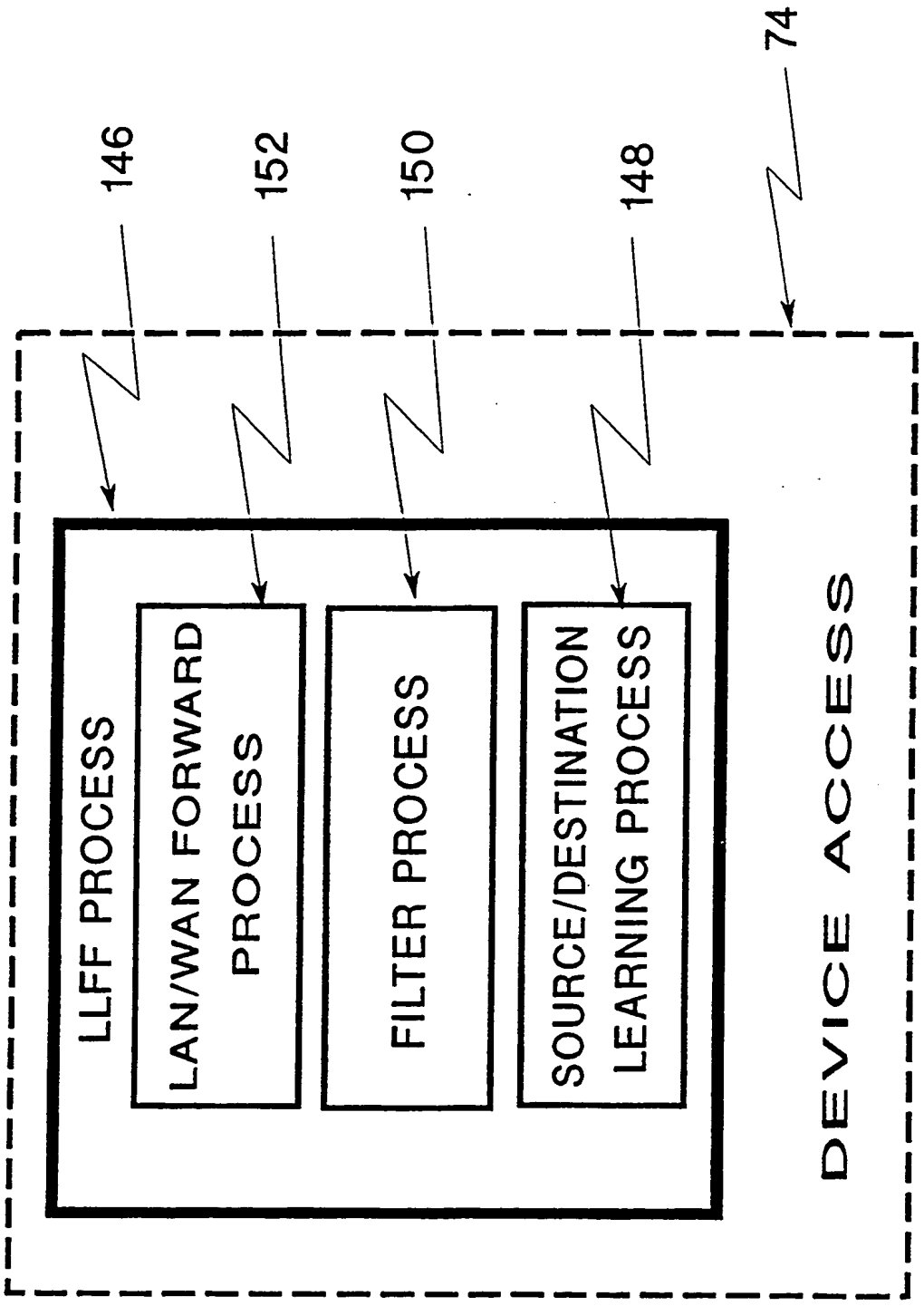

74
146
152
150
148
LLFF PROCESS
LAN/WAN FORWARD PROCESS
FILTER PROCESS
SOURCE/DESTINATION LEARNING PROCESS
DEVICE ACCESS

FIG 6

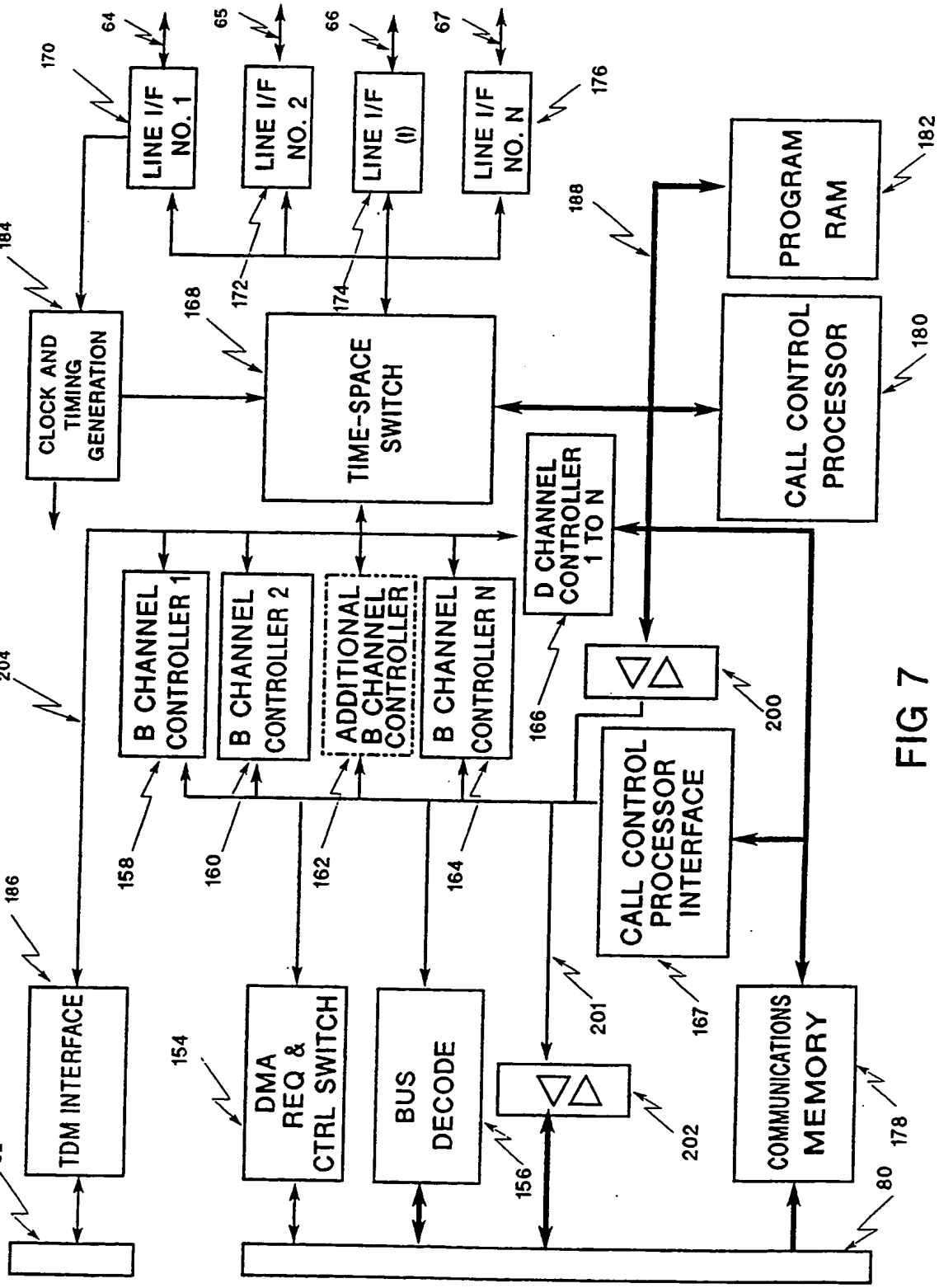

LINE I/F NO. 1
LINE I/F NO. 2
LINE I/F (I)
LINE I/F NO. N
PROGRAM RAM
CLOCK AND TIMING GENERATION
TIME-SPACE SWITCH
CALL CONTROL PROCESSOR
D CHANNEL CONTROLLER 1 TO N
B CHANNEL CONTROLLER 1
B CHANNEL CONTROLLER 2
ADDITIONAL B CHANNEL CONTROLLER
B CHANNEL CONTROLLER N
CALL CONTROL PROCESSOR INTERFACE
TDM INTERFACE
DMA REQ & CTRL SWITCH
BUS DECODE
COMMUNICATIONS MEMORY
64
65
66
67
170
176
182
184
168
172
174
188
180
166
200
204
158
160
162
164
186
201
167
154
156
202
178
82
80

FIG 7

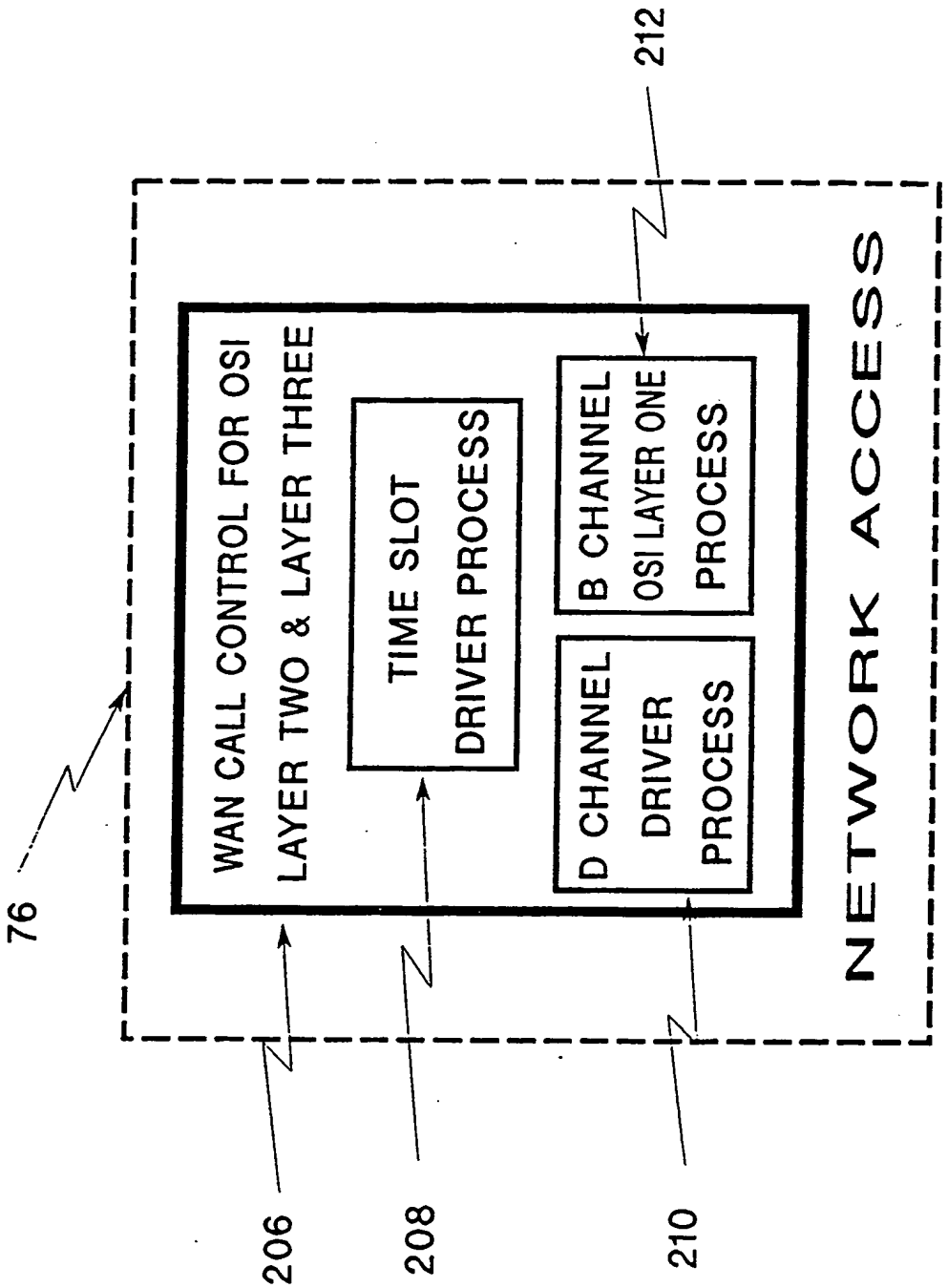

212
WAN CALL CONTROL FOR OSI
LAYER TWO & LAYER THREE
TIME SLOT
DRIVER PROCESS
B CHANNEL
OSI LAYER ONE
PROCESS
D CHANNEL
DRIVER
PROCESS
NETWORK ACCESS
76
206
208
210

FIG 8

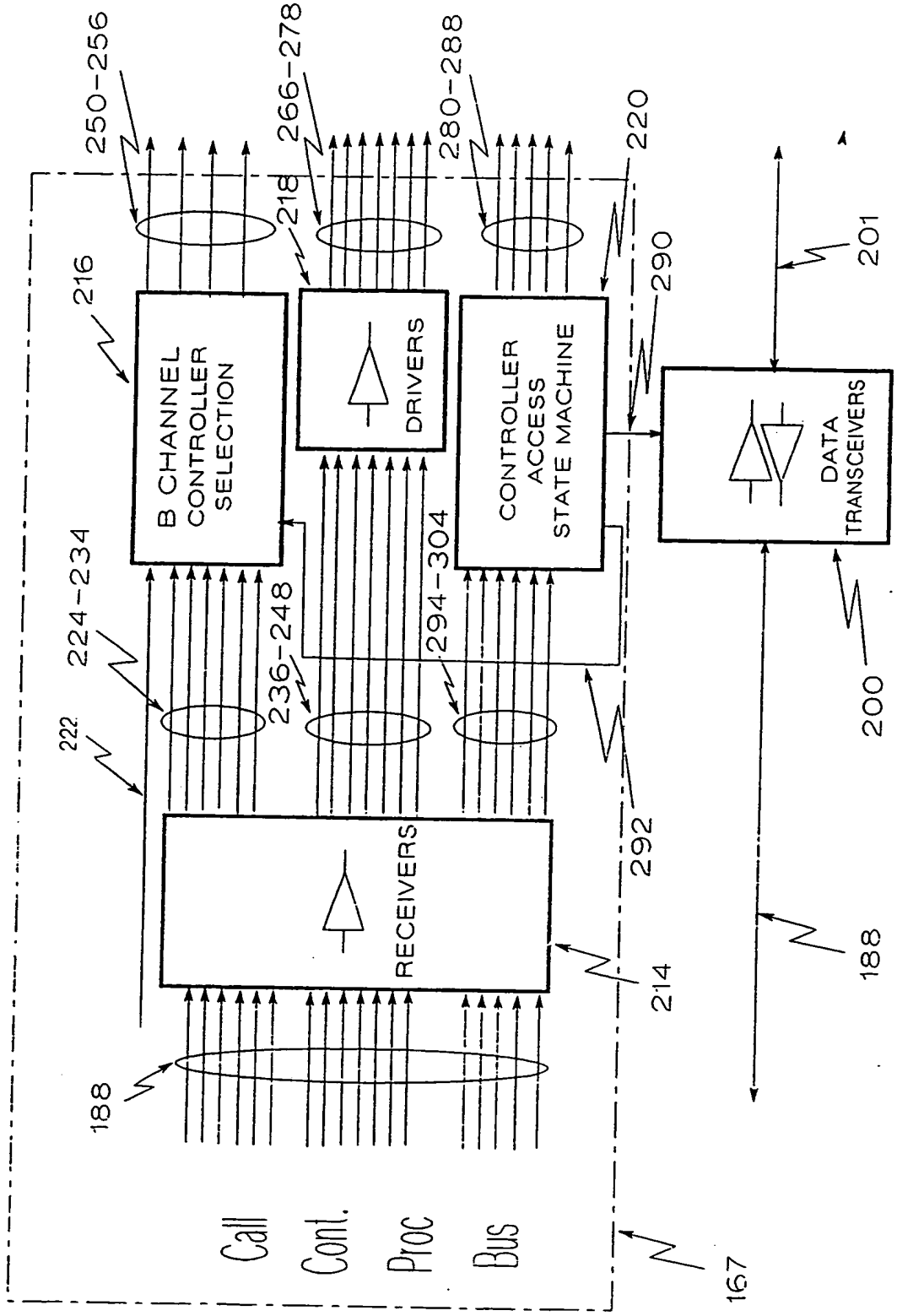

250-256
266-278
280-288
220
218
216
201
290
B CHANNEL CONTROLLER SELECTION
DRIVERS
CONTROLLER ACCESS STATE MACHINE
DATA TRANSCEIVERS
224-234
236-248
294-304
222
200
292
RECEIVERS
214
188
188
Call Cont. Proc Bus
167

FIG 9

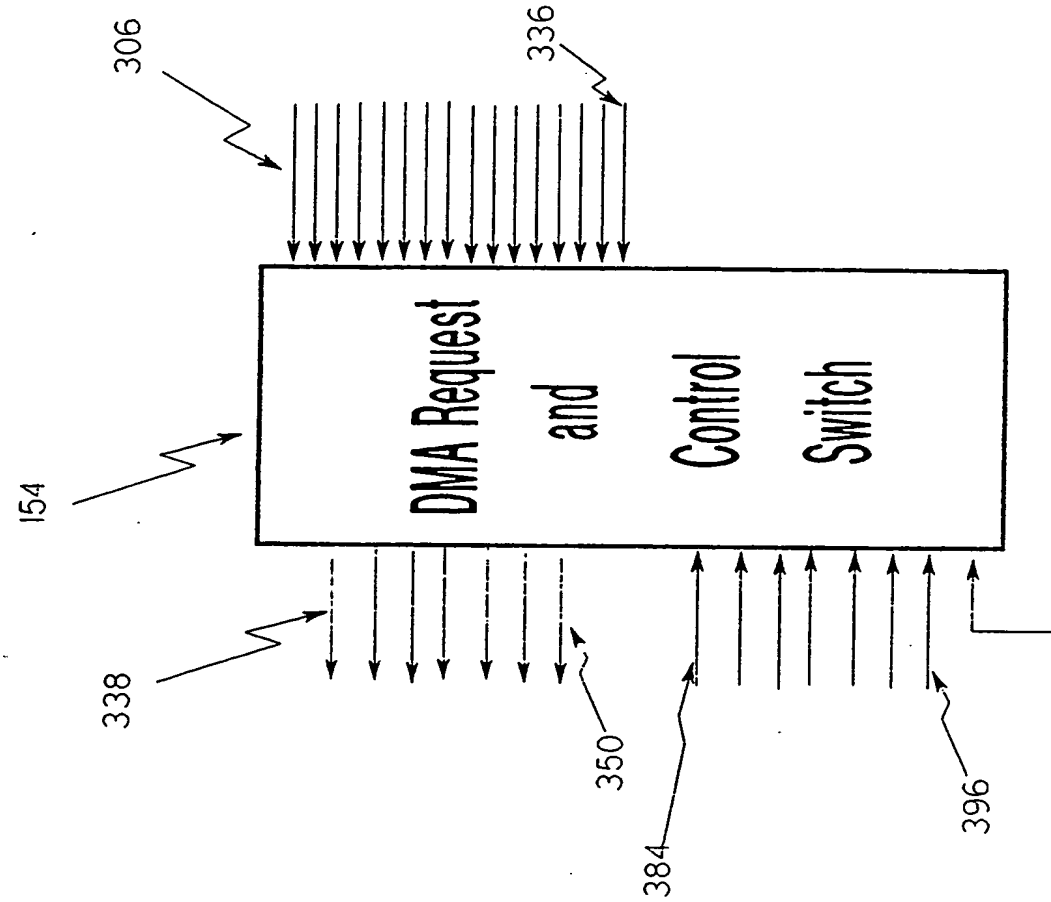

306
336
DMA Request and Control Switch
154
338
350
384
396
222

FIG. 10

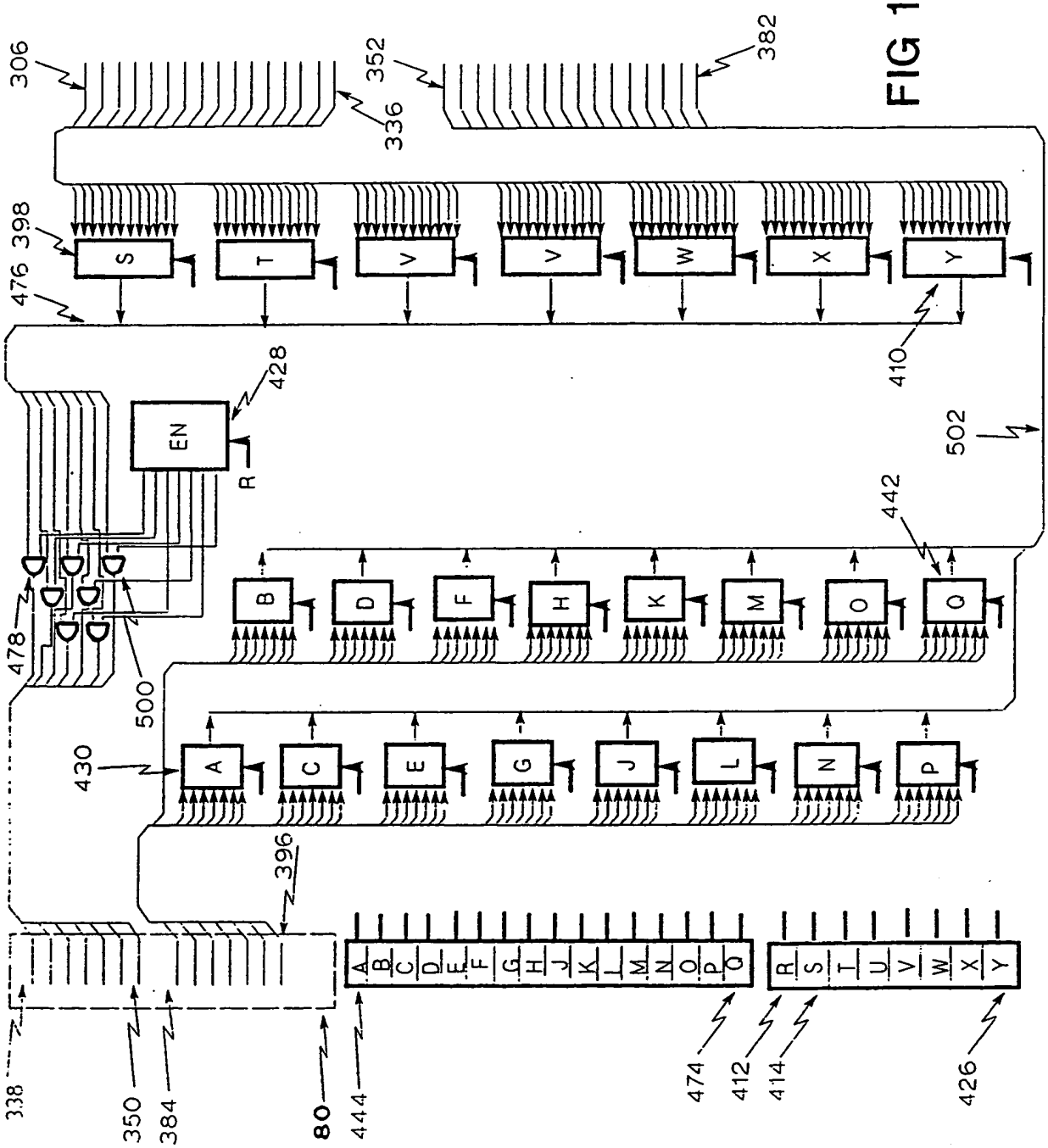

306
352
382
336
398
476
S
T
V
V
W
X
Y
410
428
EN
R
502
442
B
D
F
H
K
M
O
Q
478
500
430
A
C
E
G
J
L
N
P
396
A B C D E F G H J K L M N O P Q
R S T U V W X Y
338
350
384
80
444
474
412
414
426

FIG 11

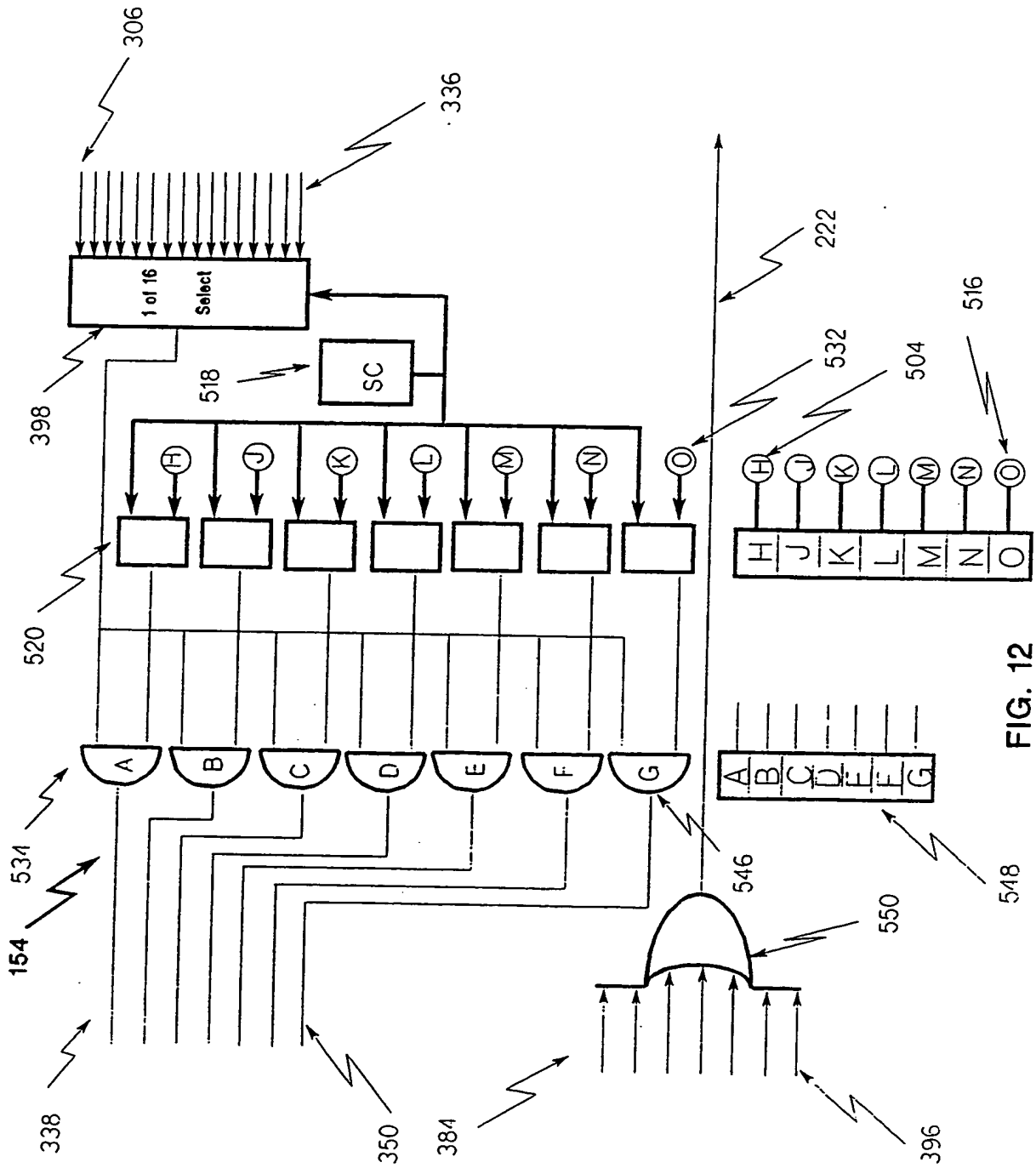
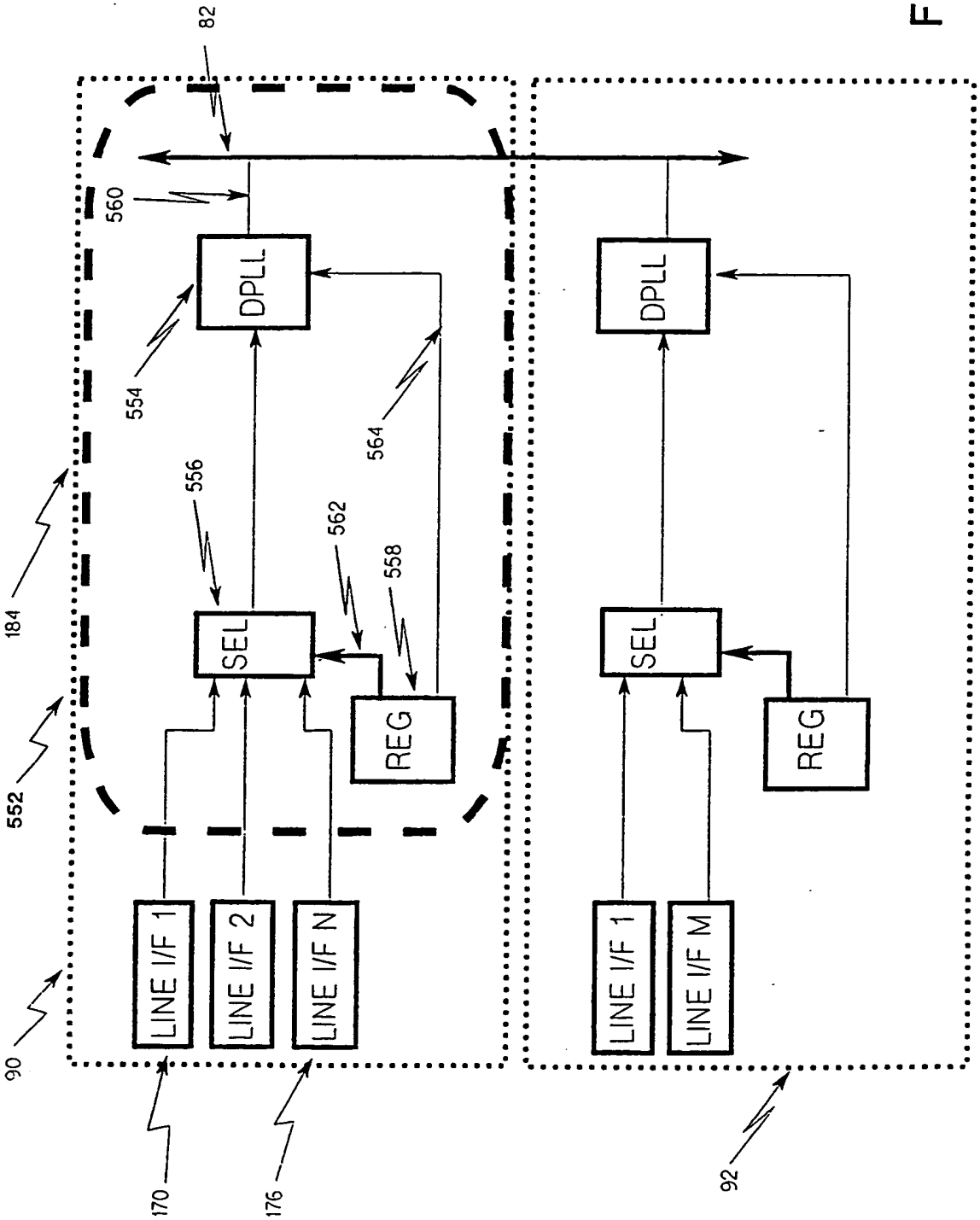

306
336
222
516
1 of 16 Select
SC
518
532
504
398
H J K L M N O
520
A B C D E F G
531
154
546
548
550
338
350
384
396

FIG. 12

FIG 13


82
560
DPLL
554
564
556
562
558
SEL
REG
184
552
LINE I/F 1
LINE I/F 2
LINE I/F N
90
170
176
DPLL
SEL
REG
LINE I/F 1
LINE I/F M
92

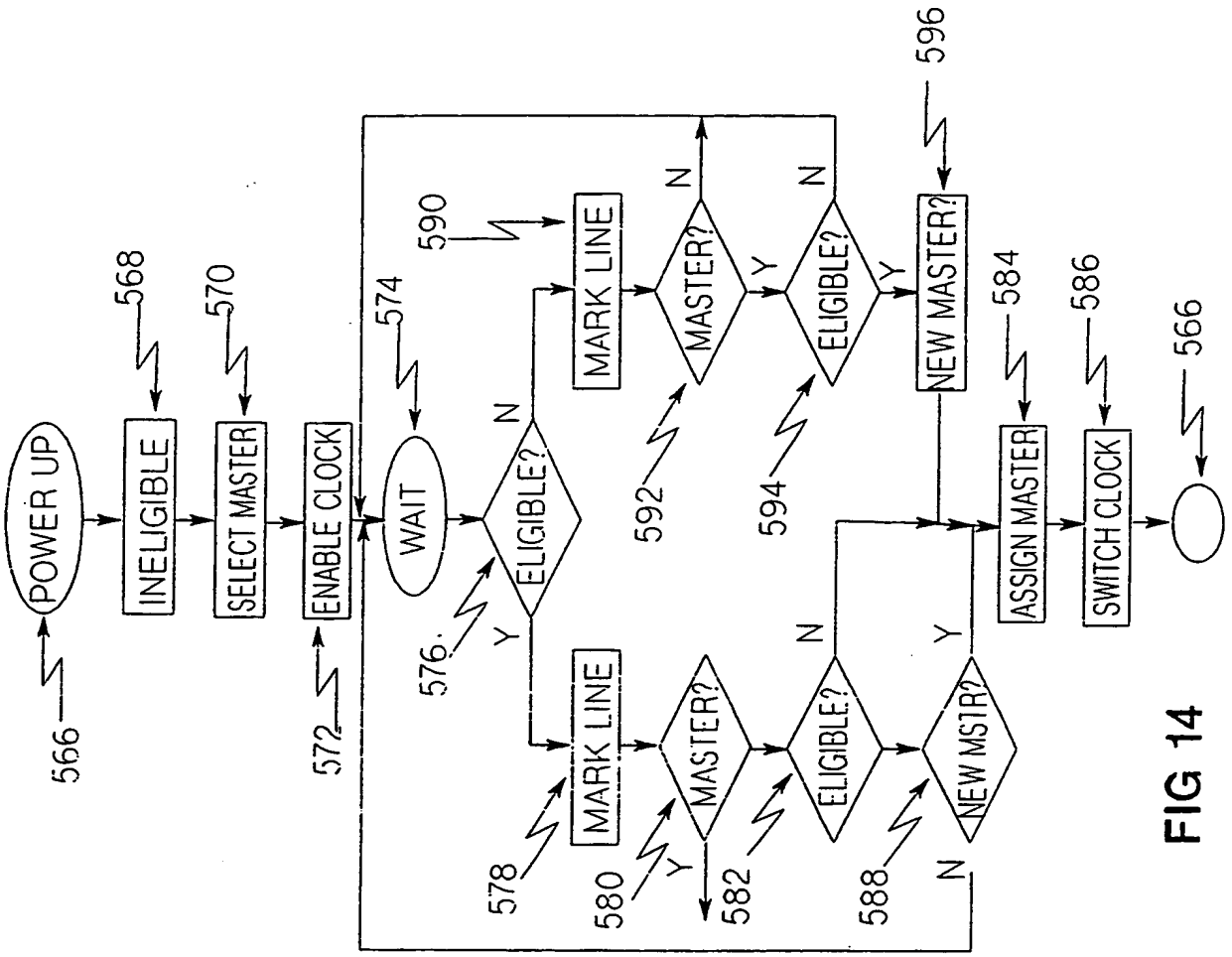

POWER UP
566
INELIGIBLE
568
SELECT MASTER
570
ENABLE CLOCK
572
WAIT
574
ELIGIBLE?
576
N
Y
MARK LINE
590
MASTER?
592
ELIGIBLE?
594
NEW MASTER?
596
MARK LINE
578
MASTER?
580
ELIGIBLE?
582
NEW MSTR?
588
ASSIGN MASTER
584
SWITCH CLOCK
586
566

FIG 14

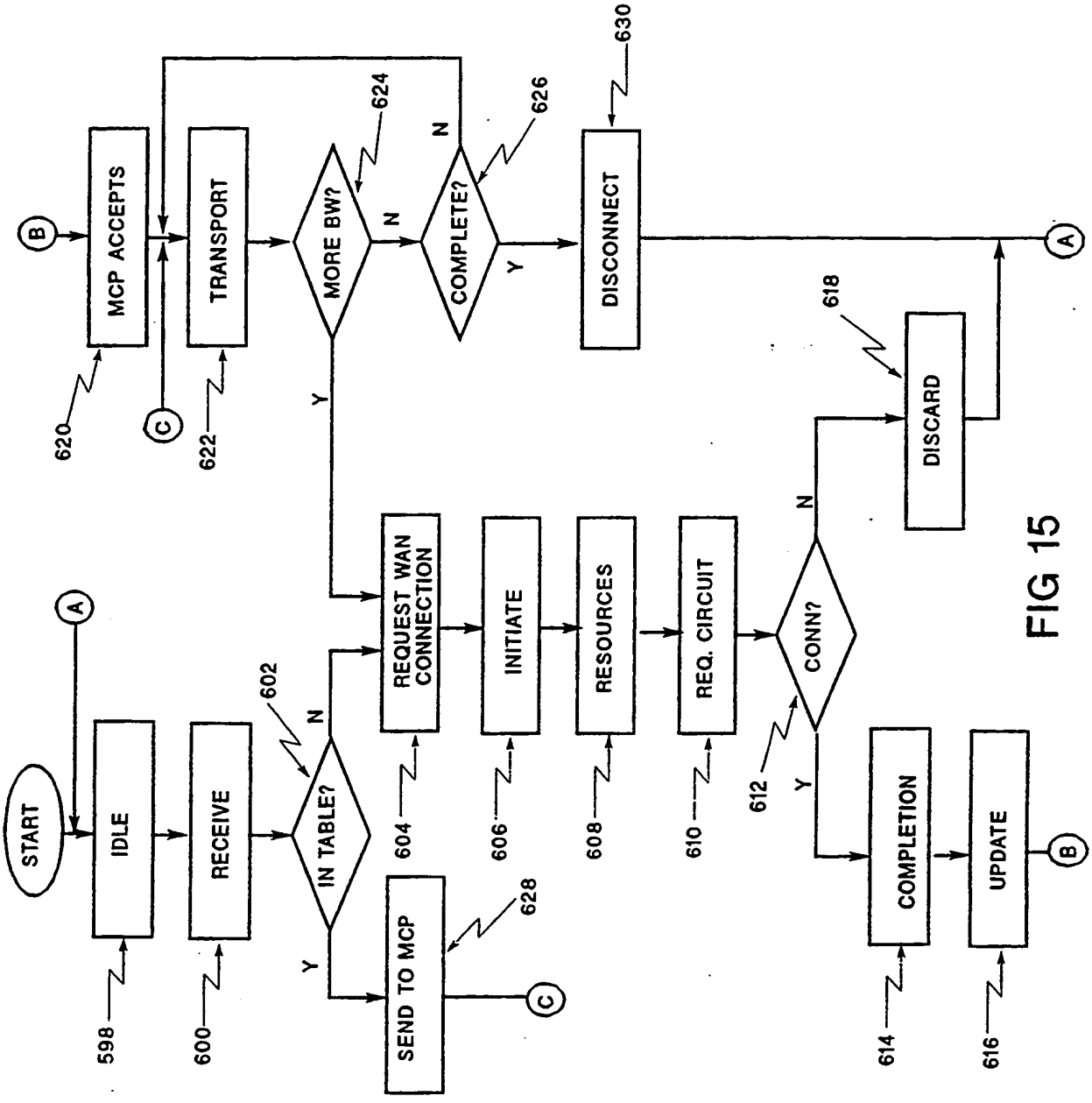

START
IDLE
RECEIVE
IN TABLE?
SEND TO MCP
REQUEST WAN CONNECTION
INITIATE
RESOURCES
REQ. CIRCUIT
CONN?
DISCARD
COMPLETION
UPDATE
MCP ACCEPTS
TRANSPORT
MORE BW?
COMPLETE?
DISCONNECT
A
B
C
Y
N
598
600
602
604
606
608
610
612
614
616
618
620
622
624
626
628
630

FIG 15

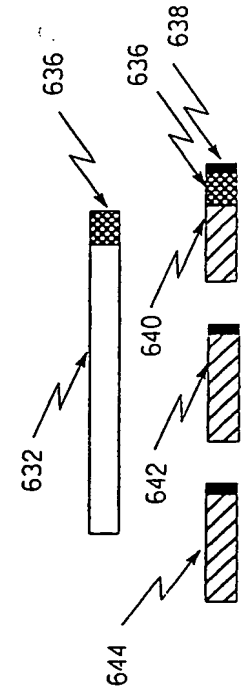


FIG 16C

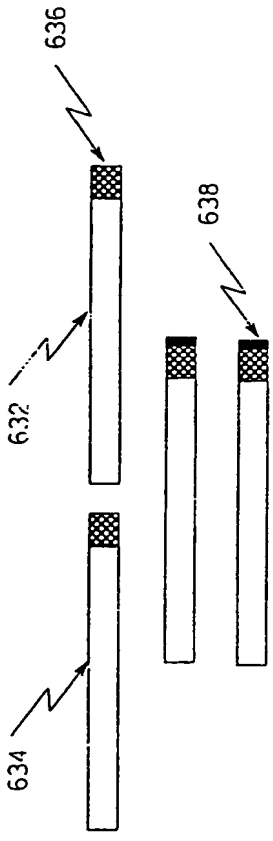


FIG 16A

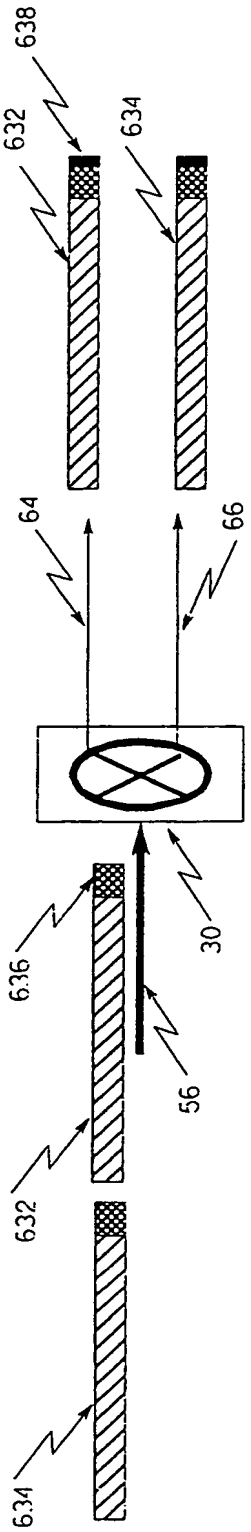


FIG 16B

FIG 16

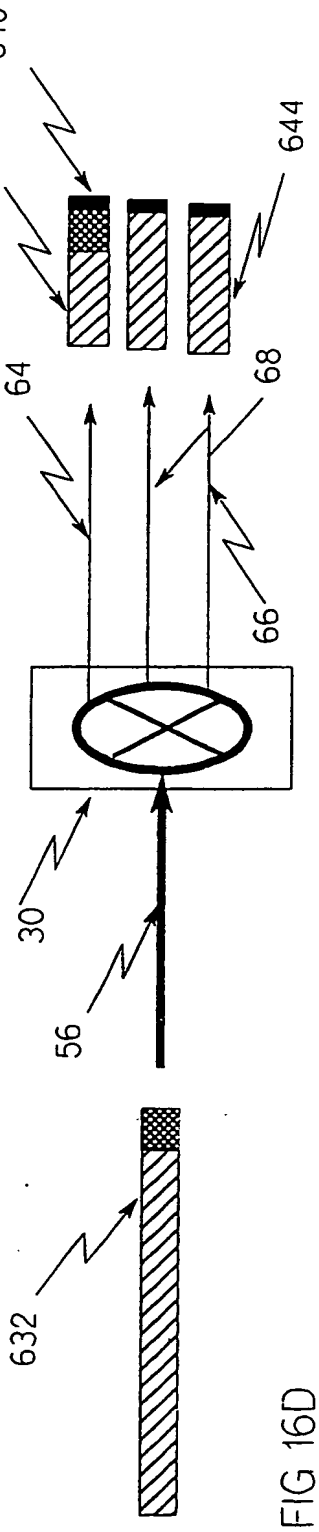


FIG 16D

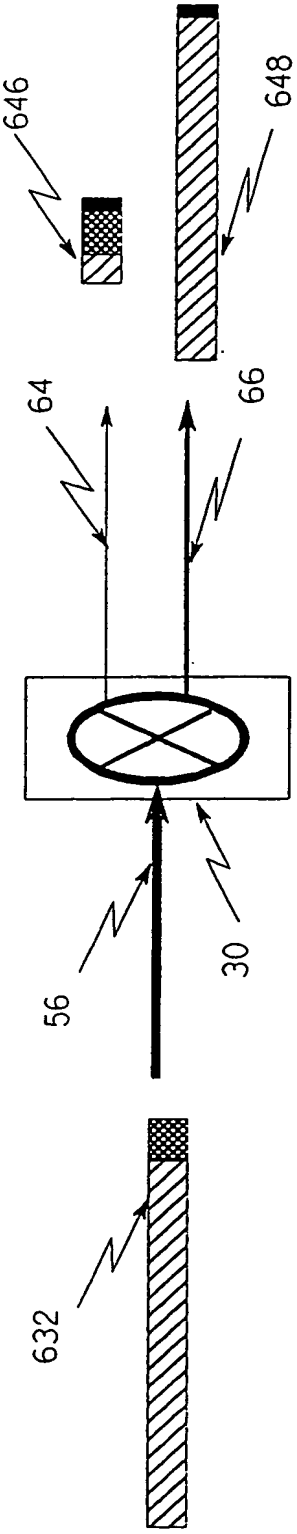


FIG 16E

FIG 16

INTERNATIONAL SEARCH REPORT

PCT/US92/11044

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H04J 3/16; H04L 12/40
US CL :370/94.1, 95.1, 112; 375/38,107
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/94.1, 95.1, 112; 375/38,107 370/60,61 68,84,85.7,103

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 5,005,170 (Nelson) 02 April 1991 See column 2, line 63 to column 3, line 25.	1-10
Y	US,A, 4,899,334 (Shimuzu) 06 February 1990 See Abstract.	1-10,15
Y	US,A, 4,899,337 (Hirai) 06 February 1990 See column 2, lines 17-40.	6-7
X Y	US,A, 4,991,172 (Cidon et al.) 05 February 1991 See column 6, lines 41-52.	11-12 13-20,22-24
Y X	US,A, 4,888,765 (Dike) 19 December 1989 See column 2, lines 8-24.	13,14,16-20 22-24

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 03 MARCH 1993	Date of mailing of the international search report 30 MAR 1993
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer Ngoc Nguyen for BENEDICT V. SAFOURE NGOC-BO TELEPHONE DIVISION Telephone No. (703) 305-4364

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/11044

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A, 4,885,738 (Bowers et al.) 05 December 1991 See Abstract.	21
Y	US,A, 4,547,880 (De Vita et al.) 15 October 1985 See figure 4, column 8, lines 24-57.	25-28
Y	US,A, 4,823,124 (Beauchemin) 18 April 1989 See figure 2, column 5, lines 23-30, column 7, line 63- column 7, line 3.	25-28
X	US,A, 5,068,877 (Near et al.) 26 November 1991 See Abstract.	29-32

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

Claims 1-24 drawn to sending high bandwidth messages over a plurality of low bandwidth channels classified in 370-112.

Claims 25-28 drawn to transferring messages between a memory and a channel classified in 370-95.1.

Claims 29-32 drawn to synchronizer classified in 375-107.

The transmission scheme of Group I does not require message transfer of Group II or the synchronizer of Group III. The message transfer of Group II and the synchronizer of Group III can be used in other than the transmission system of Group I.